LEHRBUCH

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Praktische Elektronik

Datenblätter
Analog- und CMOS-Technik

Springer Vieweg

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The CA3140 Series has the same 8-lead pinout used for the "741" and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3140AE	-55 to 125	8 Ld PDIP	E8.3
CA3140AM (3140A)	-55 to 125	8 Ld SOIC	M8.15
CA3140AS	-55 to 125	8 Pin Metal Can	T8.C
CA3140AT	-55 to 125	8 Pin Metal Can	T8.C
CA3140E	-55 to 125	8 Ld PDIP	E8.3
CA3140M (3140)	-55 to 125	8 Ld SOIC	M8.15
CA3140M96 (3140)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140T	-55 to 125	8 Pin Metal Can	T8.C

Features

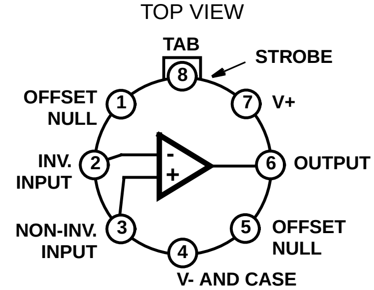
- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ)
  - Very Low Input Current (I_I) -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

Applications

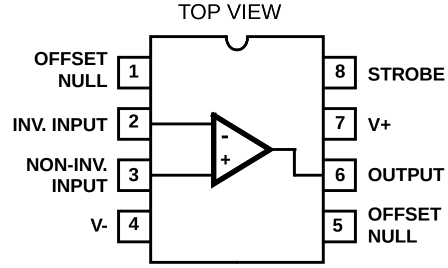
- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (µseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

Pinouts

CA3140 (METAL CAN)
TOP VIEW



CA3140 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
Differential Mode Input Voltage 8V
DC Input Voltage . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current 1mA
Output Short Circuit Duration (Note 2) . . . . Indefinite

Operating Conditions

Temperature Range . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	100	N/A
SOIC Package	160	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can Package). . . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CA3140	TYPICAL VALUES CA3140A	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}		4.7	18	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 27)	e_N	BW = 140kHz, R_S = 1MΩ		48	48	µV
Equivalent Input Noise Voltage (See Figure 35)	e_N	R_S = 100Ω	f = 1kHz	40	40	$nV/\sqrt{Hz}$
			f = 10kHz	12	12	$nV/\sqrt{Hz}$
Short Circuit Current to Opposite Supply	$I_{OM}+$		Source	40	40	mA
	$I_{OM}-$		Sink	18	18	mA
Gain-Bandwidth Product, (See Figures 6, 30)	f_T			4.5	4.5	MHz
Slew Rate, (See Figure 31)	SR			9	9	V/µs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	µA
Transient Response (See Figure 28)	t_r	R_L = 2kΩ, C_L = 100pF	Rise Time	0.08	0.08	µs
	OS		Overshoot	10	10	%
Settling Time at $10V_{P-P}$, (See Figure 5)	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	To 1mV	4.5	4.5	µs
			To 10mV	1.4	1.4	µs

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3140 MIN	CA3140 TYP	CA3140 MAX	CA3140A MIN	CA3140A TYP	CA3140A MAX	UNITS
Input Offset Voltage	$\|V_{IO}\|$	-	5	15	-	2	5	mV
Input Offset Current	$\|I_{IO}\|$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA
Large Signal Voltage Gain (Note 3) (See Figures 6, 29)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB

Electrical Specifications

For Equipment Design, at V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CA3140 MIN	CA3140 TYP	CA3140 MAX	CA3140A MIN	CA3140A TYP	CA3140A MAX	UNITS
Common Mode Rejection Ratio (See Figure 34)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36)	PSRR	-	100	150	-	100	150	µV/V
		76	80	-	76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	$V_{OM}+$	+12	13	-	+12	13	-	V
	$V_{OM}-$	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 32)	I+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	µV/°C

NOTES:

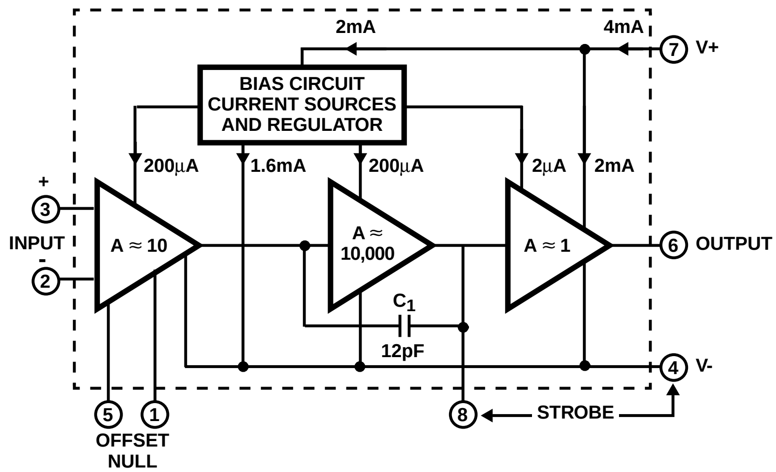
3. At V_O = 26V_{P-P}, +12V, -14V and R_L = 2kΩ.
4. At R_L = 2kΩ.

Electrical Specifications

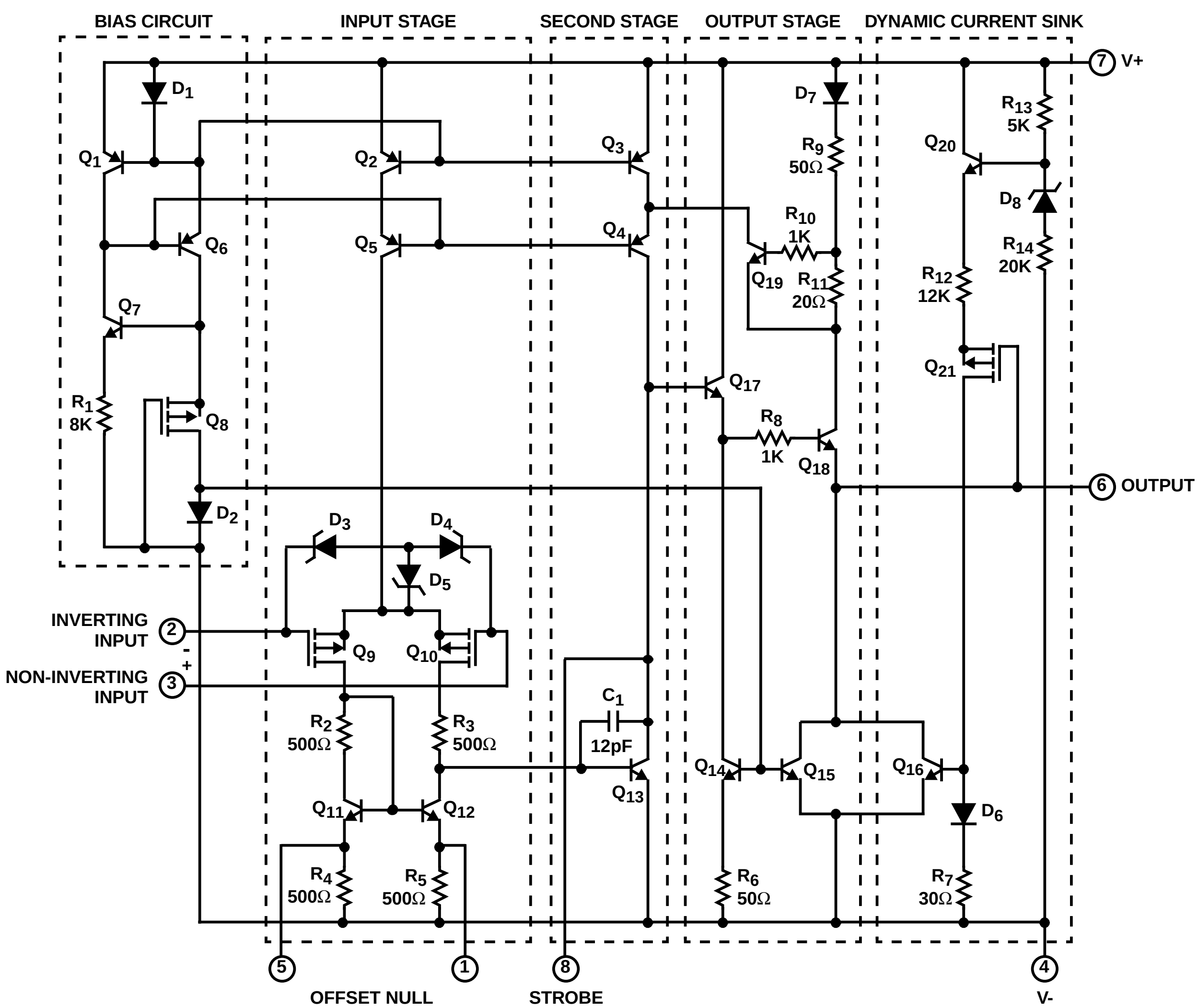
For Design Guidance At V+ = 5V, V- = 0V, T_A = 25°C

PARAMETER		SYMBOL	TYPICAL VALUES CA3140	TYPICAL VALUES CA3140A	UNITS
Input Offset Voltage		$\lvert V_{IO}\rvert$	5	2	mV
Input Offset Current		$\lvert I_{IO}\rvert$	0.1	0.1	pA
Input Current		I_I	2	2	pA
Input Resistance		R_I	1	1	TΩ
Large Signal Voltage Gain (See Figures 6, 29)		A_{OL}	100	100	kV/V
			100	100	dB
Common Mode Rejection Ratio		CMRR	32	32	µV/V
			90	90	dB
Common Mode Input Voltage Range (See Figure 8)		V_{ICR}	-0.5	-0.5	V
			2.6	2.6	V
Power Supply Rejection Ratio		PSRR $\Delta V_{IO}/\Delta V_S$	100	100	µV/V
			80	80	dB
Maximum Output Voltage (See Figures 2, 8)		$V_{OM}+$	3	3	V
		$V_{OM}-$	0.13	0.13	V
Maximum Output Current:	Source	$I_{OM}+$	10	10	mA
	Sink	$I_{OM}-$	1	1	mA
Slew Rate (See Figure 31)		SR	7	7	V/µs
Gain-Bandwidth Product (See Figure 30)		f_T	3.7	3.7	MHz
Supply Current (See Figure 32)		I+	1.6	1.6	mA
Device Dissipation		P_D	8	8	mW
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low			200	200	µA

Block Diagram



Schematic Diagram



NOTE: All resistance values are in ohms.

Application Information

Circuit Description

As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The CA3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

Input Stage

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q_9, Q_{10}) working into a mirror pair of bipolar transistors (Q_{11}, Q_{12}) functioning as load resistors together with resistors R_2 through R_5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q_{13}). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across Terminals 1 and 5 and with its slider arm connected to Terminal 4. Cascode-connected bipolar transistors Q_2, Q_5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D_3, D_4, D_5 provide gate oxide protection against high voltage transients, e.g., static electricity.

Second Stage

Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q_{13} and its cascode connected load resistance provided by bipolar transistors Q_3, Q_4. On-chip phase compensation, sufficient for a majority of the applications is provided by C_1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output Terminal 6 swings low, i.e., approximately to Terminal 4 potential.

Output Stage

The CA3140 Series circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q_{17}, Q_{18}) is established by transistors (Q_{14}, Q_{15}) whose base currents are “mirrored” to current flowing through diode D_2 in the bias circuit section. When the CA3140 is operating such that output Terminal 6 is sourcing current, transistor Q_{18} functions as an emitter-follower to source current from the V+ bus (Terminal 7), via D_7, R_9, and R_{11}. Under these conditions, the collector potential of Q_{13} is sufficiently high to permit the necessary flow of base current to emitter follower Q_{17} which, in turn, drives Q_{18}.

When the CA3140 is operating such that output Terminal 6 is sinking current to the V- bus, transistor Q_{16} is the current sinking element. Transistor Q_{16} is mirror connected to D_6, R_7, with current fed by way of Q_{21}, R_{12}, and Q_{20}. Transistor Q_{20}, in turn, is biased by current flow through R_{13}, zener D_8, and R_{14}. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output Terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q_{13} is driven below its quiescent level, thereby causing Q_{17}, Q_{18} to decrease the output voltage at Terminal 6. Thus, the gate terminal of PMOS transistor Q_{21} is displaced toward the V- bus, thereby reducing the channel resistance of Q_{21}. As a consequence, there is an incremental increase in current flow through Q_{20}, R_{12}, Q_{21}, D_6, R_7, and the base of Q_{16}. As a result, Q_{16} sinks current from Terminal 6 in direct response to the incremental change in output voltage caused by Q_{18}. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q_{18}. Short circuit protection of the output circuit is provided by Q_{19}, which is driven into conduction by the high voltage drop developed across R_{11} under output short circuit conditions. Under these conditions, the collector of Q_{19} diverts current from Q_4 so as to reduce the base current drive from Q_{17}, thereby limiting current flow in Q_{18} to the short circuited load terminal.

Bias Circuit

Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R_1. The function of the bias circuit is to establish and maintain constant current flow through D_1, Q_6, Q_8 and D_2. D_1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q_1, Q_2, and Q_3. D_1 may be considered as a current sampling diode that senses the emitter current of Q_6 and automatically adjusts the base current of Q_6 (via Q_1) to maintain a constant current through Q_6, Q_8, D_2. The base currents in Q_2, Q_3 are also determined by constant current flow D_1. Furthermore, current in diode connected transistor Q_2 establishes the currents in transistors Q_{14} and Q_{15}.

Typical Applications

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the CA3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, such as, for example, where one input is driven below the potential of Terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to Terminal 8 as shown in Figure 1. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

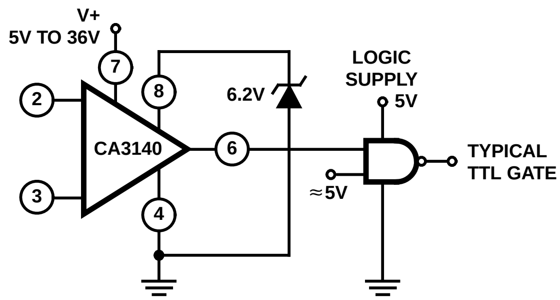


FIGURE 1. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT CA3140 OUTPUT SWING TO TTL LEVELS

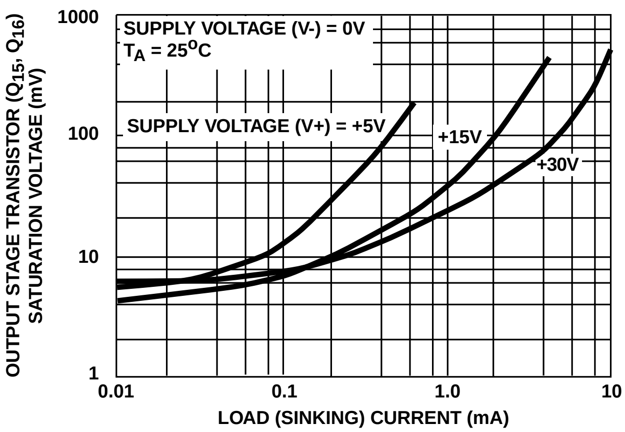


FIGURE 2. VOLTAGE ACROSS OUTPUT TRANSISTORS (Q_{15} AND Q_{16}) vs LOAD CURRENT

Figure 2 shows output current sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 4 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 3A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 3B, to optimize its utilization range are given in the Electrical Specifications table.

An alternate system is shown in Figure 3C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the voltage at Terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 8 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

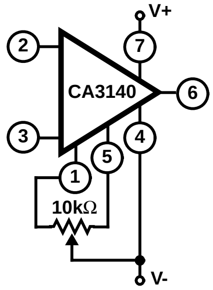


FIGURE 3A. BASIC

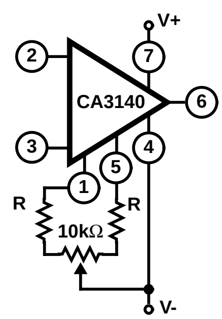


FIGURE 3B. IMPROVED RESOLUTION

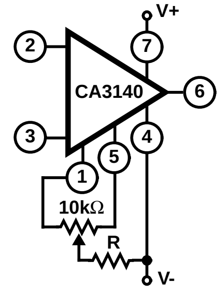


FIGURE 3C. SIMPLER IMPROVED RESOLUTION

FIGURE 3. THREE OFFSET VOLTAGE NULLING METHODS

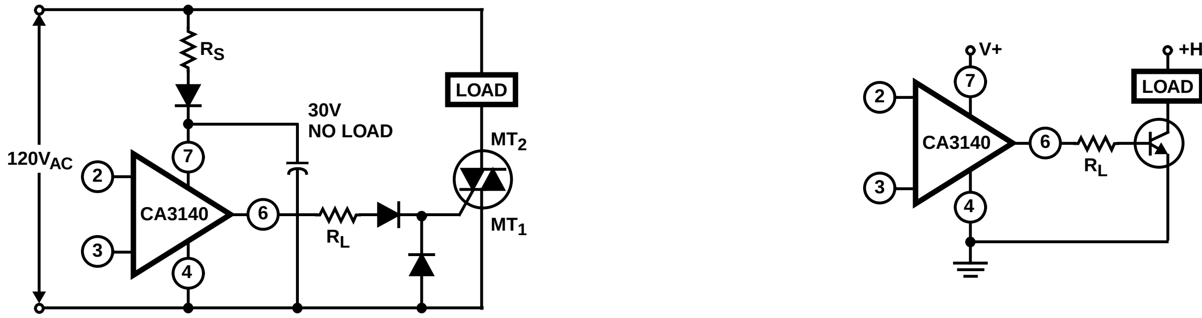


FIGURE 4. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE CA3140 SERIES

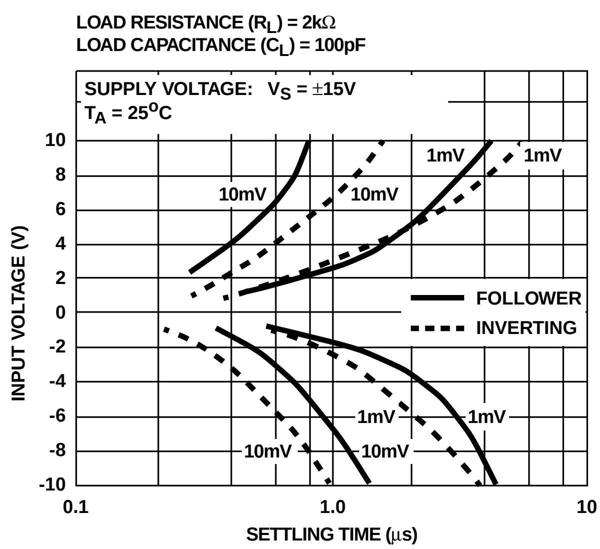


FIGURE 5A. WAVEFORM

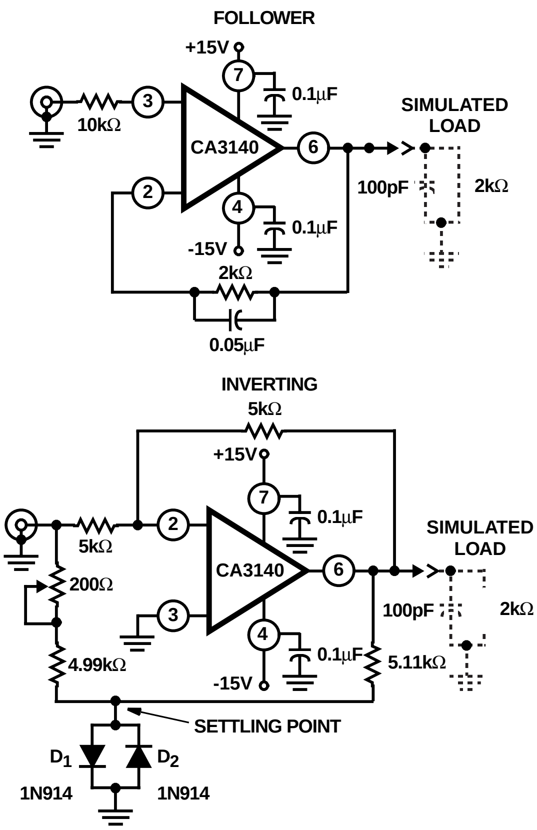


FIGURE 5B. TEST CIRCUITS

FIGURE 5. SETTLING TIME vs INPUT VOLTAGE

Bandwidth and Slew Rate

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between Terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 5 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Figure 6.

Input Circuit Considerations

As mentioned previously, the amplifier inputs can be driven below the Terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and directly driving the internal constant current source which could result in positive feedback via the output terminal. A 3.9kΩ resistor is sufficient.

The typical input current is on the order of 10pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Figure 7 shows typical input terminal current versus ambient temperature for the CA3140.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Figure 9 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for metal can); at lower temperatures (metal can and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

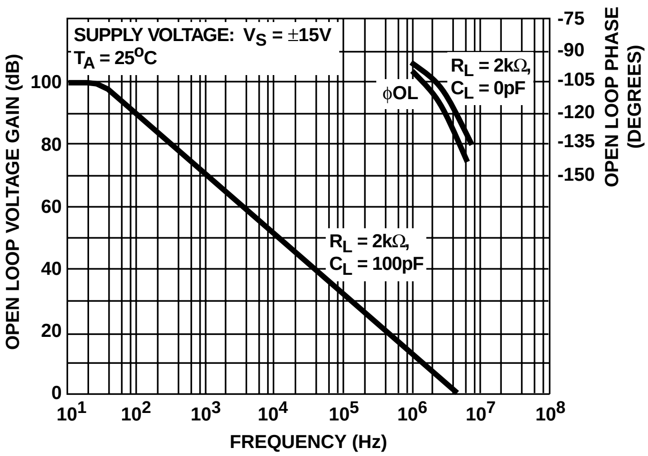


FIGURE 6. OPEN LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY

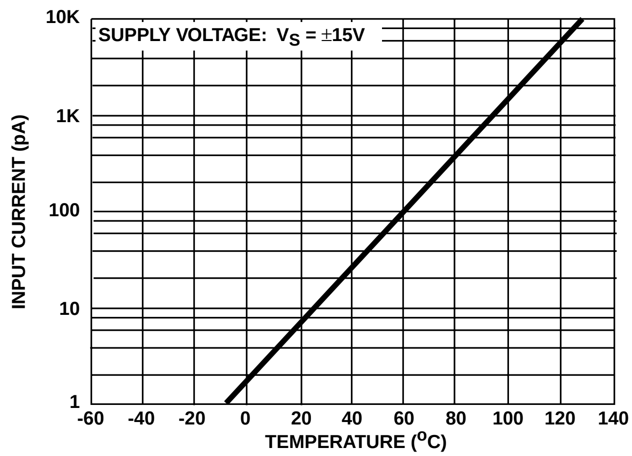


FIGURE 7. INPUT CURRENT vs TEMPERATURE

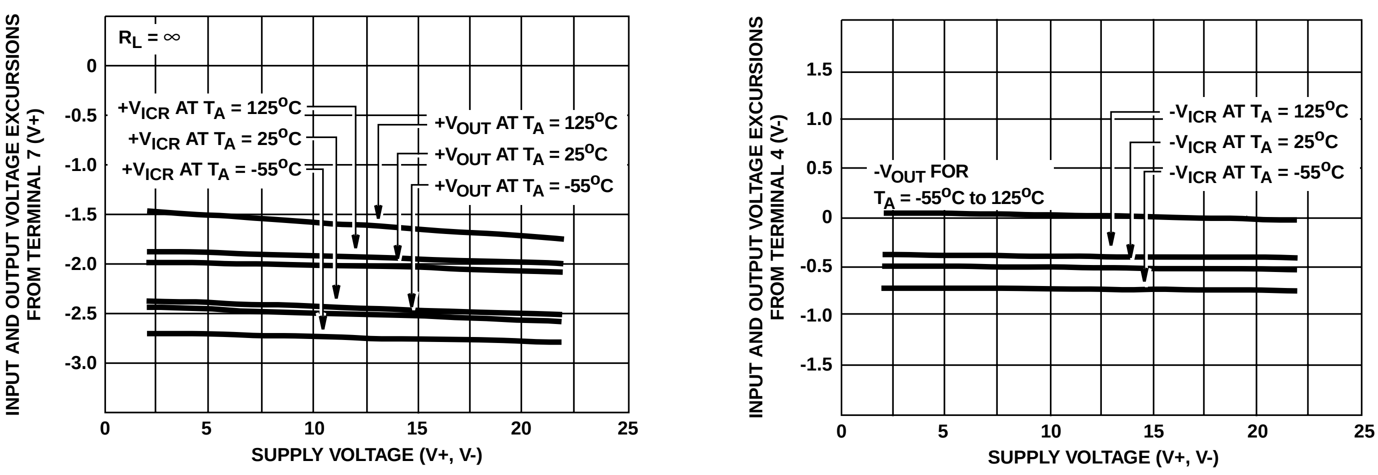


FIGURE 8. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

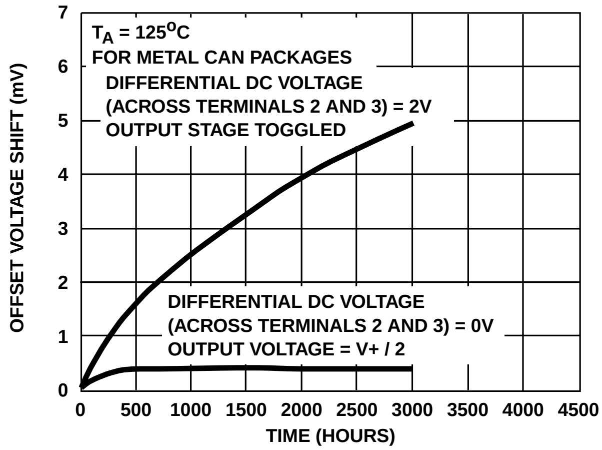


FIGURE 9. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Super Sweep Function Generator

A function generator having a wide tuning range is shown in Figure 10. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting readout amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop

The triangular output level is determined by the four 1N914 level limiting diodes of the second CA3080 and the resistor divider network connected to Terminal No. 2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High frequency ramp linearity is adjusted by the single 7pF to 60pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current generator function.

Meter Driver and Buffer Amplifier

Figure 11 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generator's frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60mV change in the applied voltage, V_{ABC} (voltage between Terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary. Two adjustments are used for the meter. The meter sensitivity control sets the meter scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects $^1/_6$ of full scale for each decade change in frequency.

Sine Wave Shaper

The circuit shown in Figure 12 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero crossing slope is established by the 10kΩ potentiometer connected between Terminals 2 and 6 of the CA3140 and the 9.1kΩ resistor and 10kΩ potentiometer from Terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

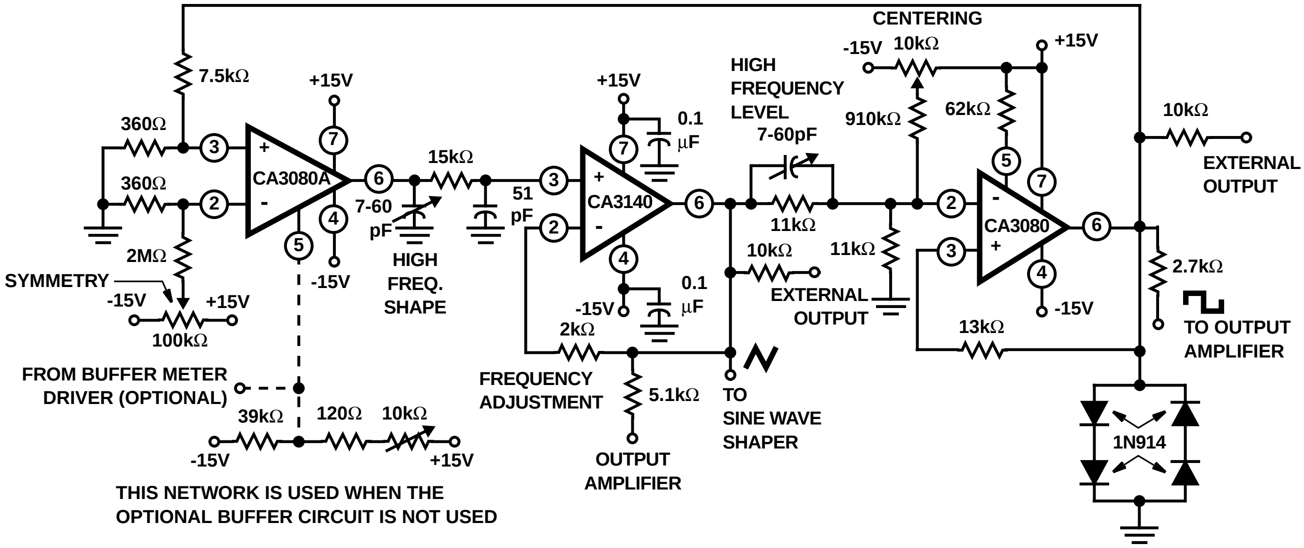
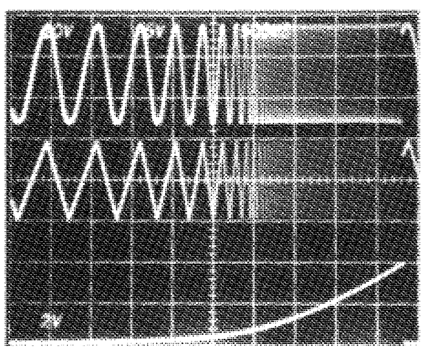


FIGURE 10A. CIRCUIT

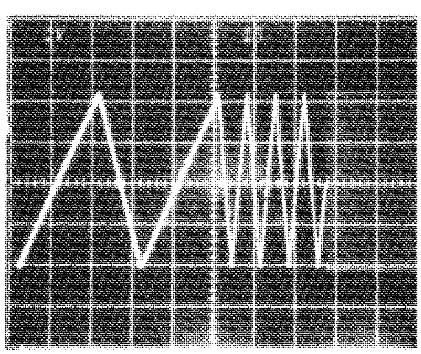


Top Trace: Output at junction of 2.7Ω and 51Ω resistors; 5V/Div., 500ms/Div.

Center Trace: External output of triangular function generator; 2V/Div., 500ms/Div.

Bottom Trace: Output of “Log” generator; 10V/Div., 500ms/Div.

FIGURE 10B. FIGURE FUNCTION GENERATOR SWEEPING



1V/Div., 1s/Div.

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the PC board and component leakages at the 100pA level.

FIGURE 10C. FUNCTION GENERATOR WITH FIXED FREQUENCIES

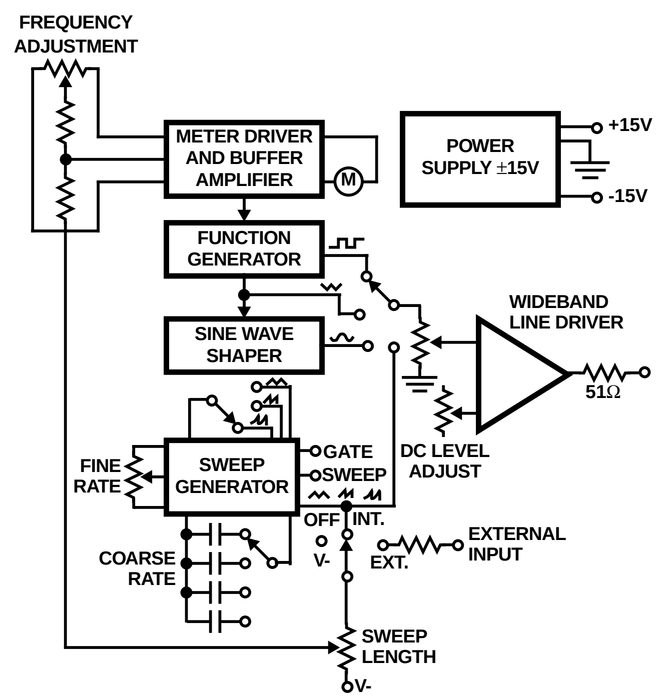


FIGURE 10D. INTERCONNECTIONS

FIGURE 10. FUNCTION GENERATOR

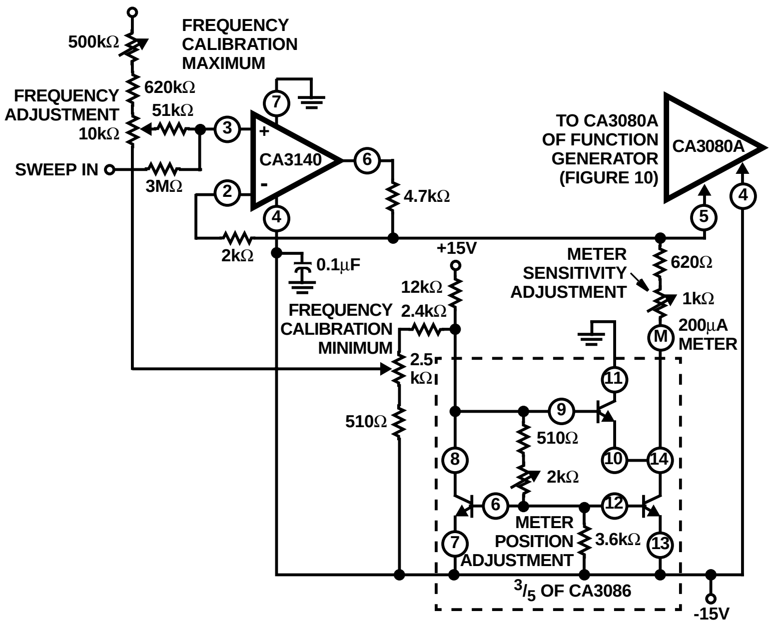


FIGURE 11. METER DRIVER AND BUFFER AMPLIFIER

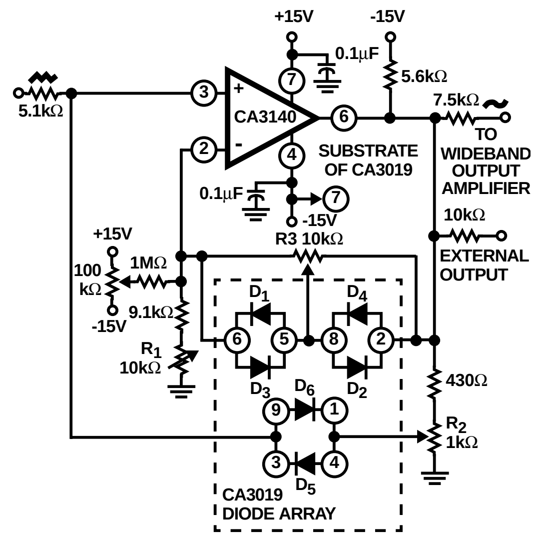


FIGURE 12. SINE WAVE SHAPER

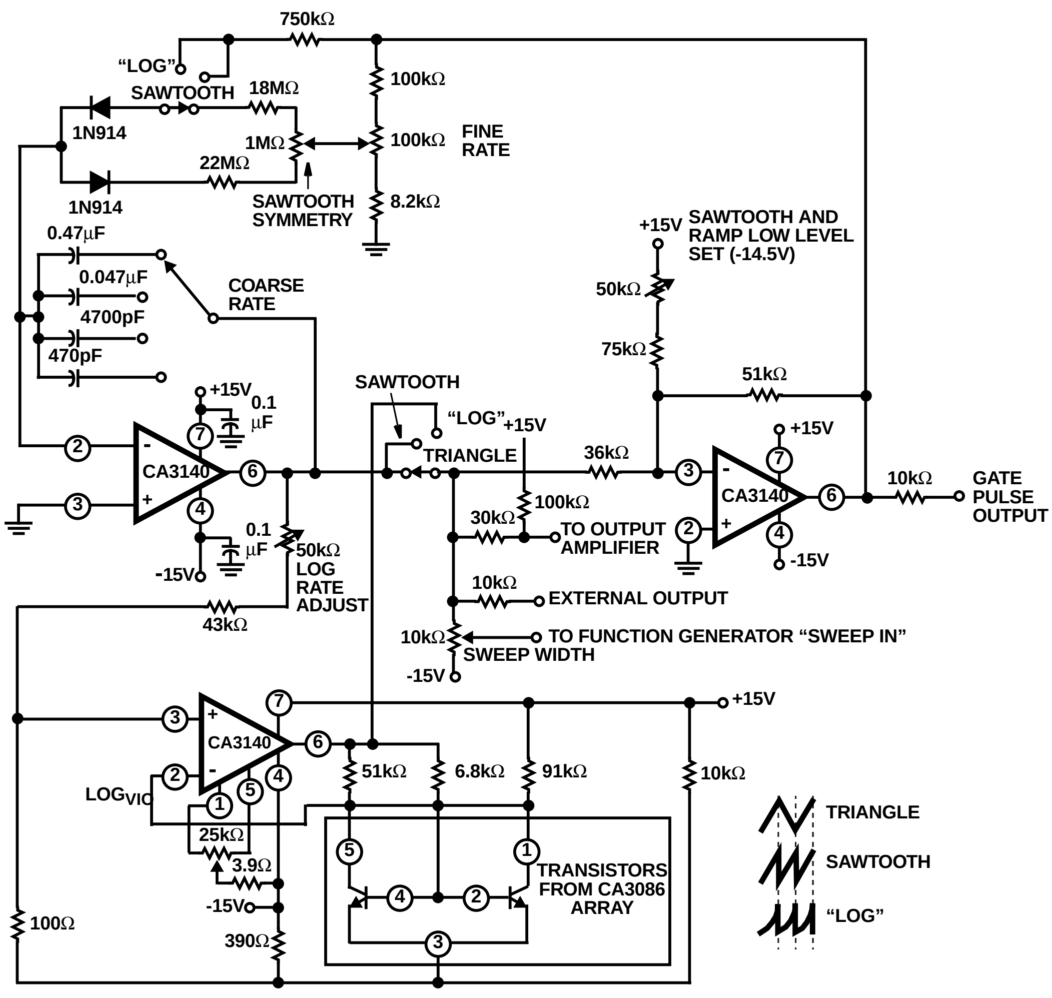


FIGURE 13. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

Sweeping Generator

Figure 13 shows a sweeping generator. Three CA3140s are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

Wideband Output Amplifier

Figure 14 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 10 and 12 provides $18V_{P-P}$ output open circuited, or $9V_{P-P}$ output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs ($18V_{P-P}$ x π x 0.5MHz).

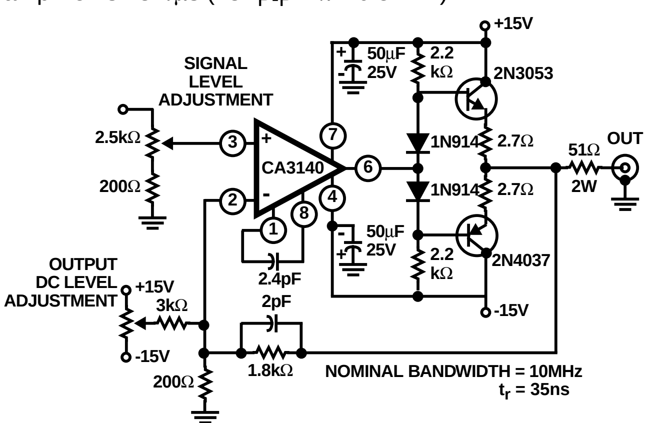


FIGURE 14. WIDEBAND OUTPUT AMPLIFIER

Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in connection with the CA3140 (see Figure 15).

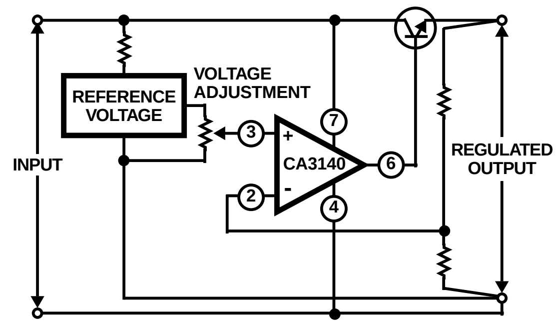


FIGURE 15. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 16 and 17, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CESAT}) across the output of the CA3140 (see Figure 2). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by Terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply rail.

Figures 16 and 17, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a metal can with heatsink), is used as the series pass element for the conventional current limiting system, Figure 16, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 17, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

Both regulators provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200µV as read with a meter having a 10MHz bandwidth.

Figure 18A shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 18B shows the transient response of the regulator with the switching of a 20Ω load at 20V output.

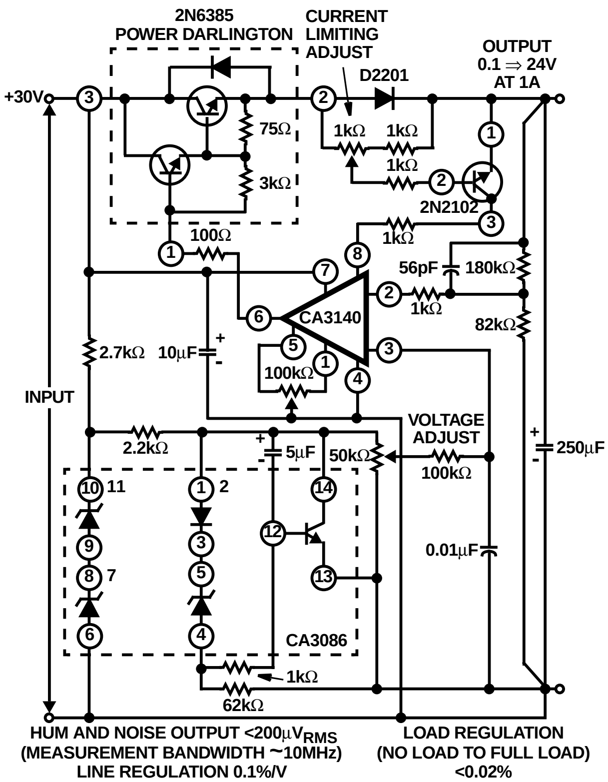


FIGURE 16. REGULATED POWER SUPPLY

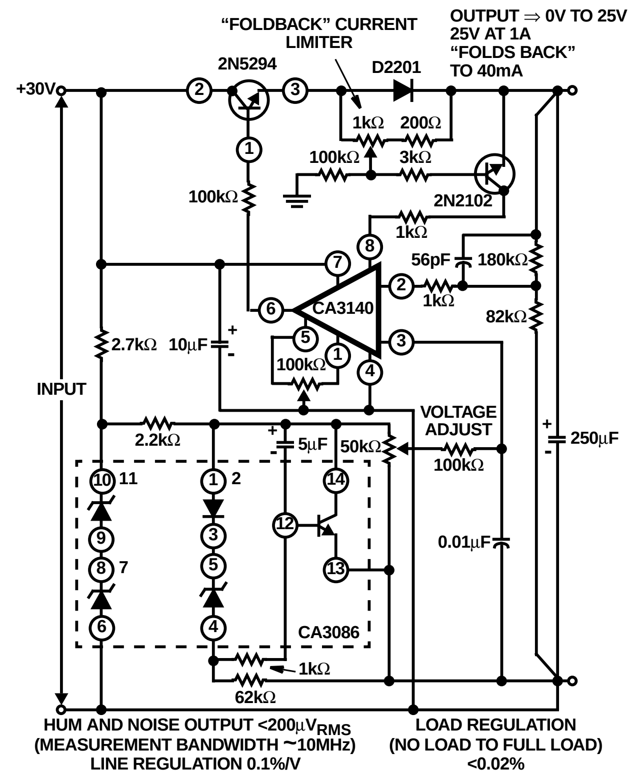
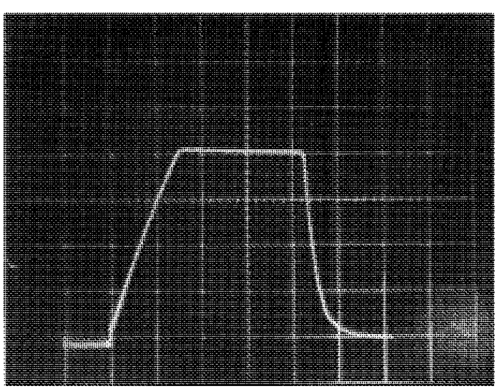
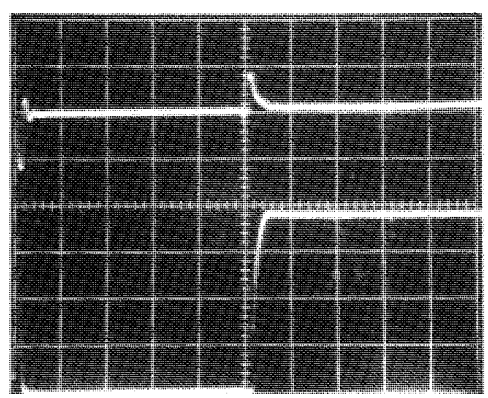


FIGURE 17. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING



5V/Div., 1s/Div.

FIGURE 18A. SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS



Top Trace: Output Voltage; 200mV/Div., 5µs/Div.

Bottom Trace: Collector of load switching transistor, load = 1A; 5V/Div., 5µs/Div.

FIGURE 18B. TRANSIENT RESPONSE

FIGURE 18. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 16 AND 17

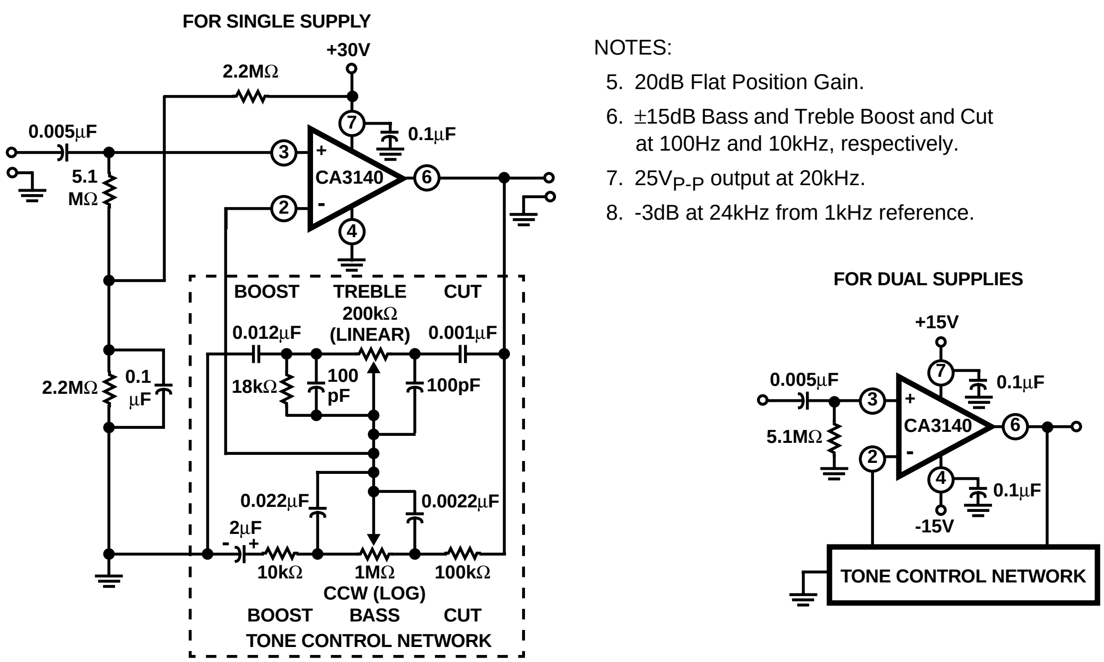
Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figures 19 and 20.

The first circuit, shown in Figure 20, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

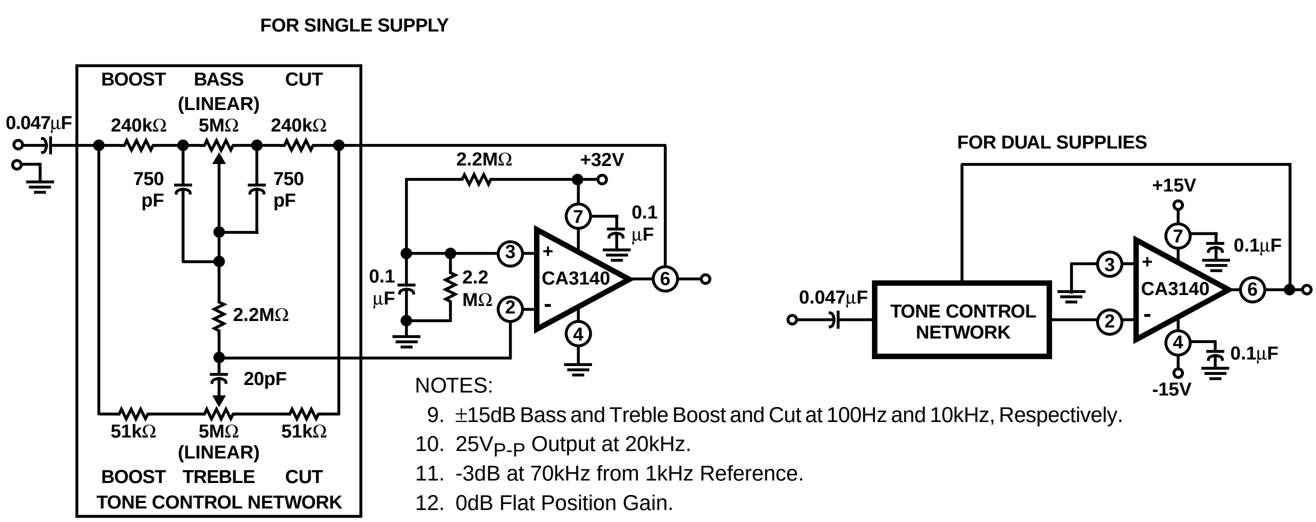
Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the CA3140. The amplifier gain is 3dB down from its "flat" position at 70kHz.

Figure 19 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from Terminal No. 3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.



NOTES:
5. 20dB Flat Position Gain.
6. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, respectively.
7. $25V_{P-P}$ output at 20kHz.
8. -3dB at 24kHz from 1kHz reference.

FIGURE 19. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)

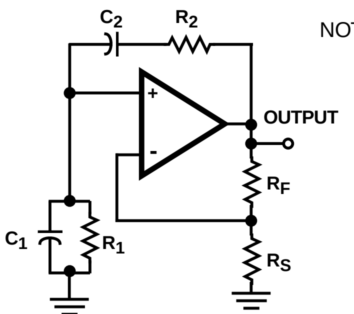


NOTES:
9. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, Respectively.
10. $25V_{P-P}$ Output at 20kHz.
11. -3dB at 70kHz from 1kHz Reference.
12. 0dB Flat Position Gain.

FIGURE 20. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES

Wien Bridge Oscillator

Another application of the CA3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 21. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/(2\pi RC)$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the CA3140.



NOTES:

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$A_{OSC} = 1 + \frac{C_1}{C_2} + \frac{R_2}{R_1}$$

$$A_{CL} = 1 + \frac{R_F}{R_S}$$

FIGURE 21. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance increases as the output amplitude is increased are a few of the elements often utilized.

Figure 22 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_F of Figure 21). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate of approximately 9V/µs when its amplitude is $16V_{P-P}$.

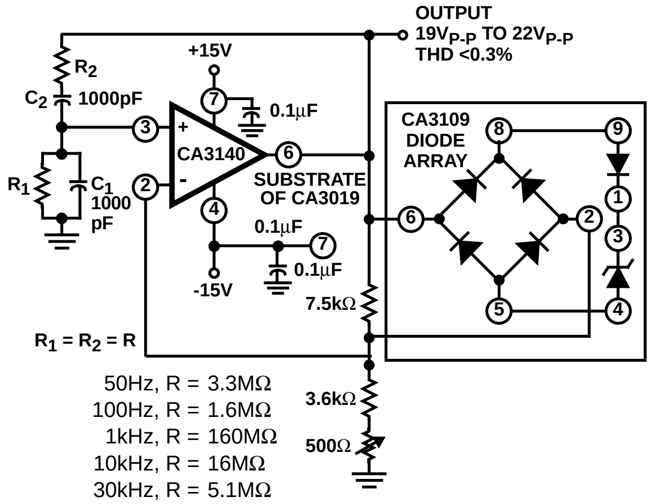


FIGURE 22. WIEN BRIDGE OSCILLATOR CIRCUIT USING CA3140

Simple Sample-and-Hold System

Figure 23 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch (see Note 13). System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

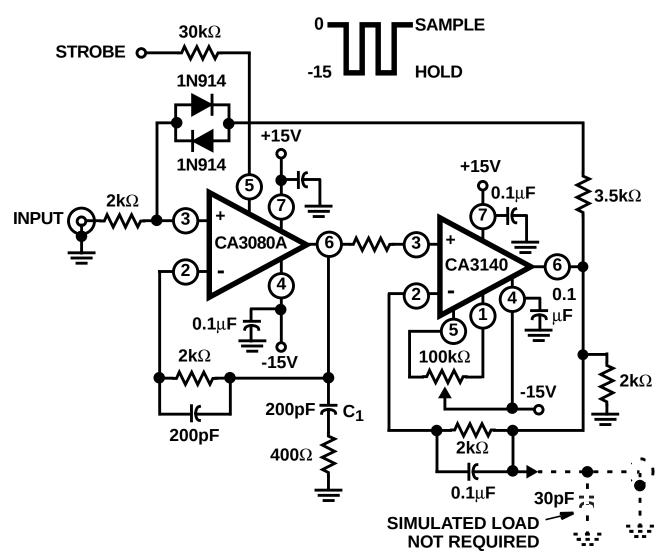


FIGURE 23. SAMPLE AND HOLD CIRCUIT

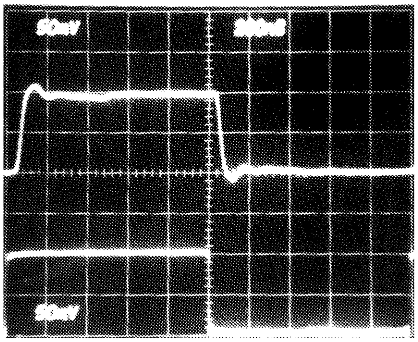
In this circuit, the storage compensation capacitance (C_1) is only 200pF. Larger value capacitors provide longer “hold” periods but with slower slew rates. The slew rate is:

$$\frac{dv}{dt} = \frac{I}{C} = 0.5\text{mA}/200\text{pF} = 2.5\text{V}/\mu\text{s}$$

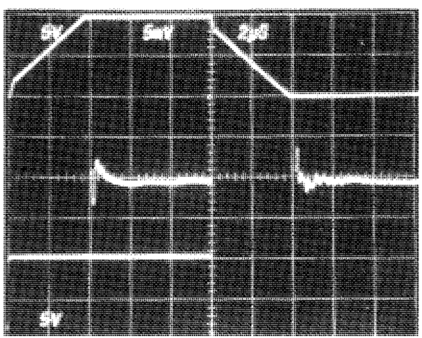
NOTE:

13. AN6668 “Applications of the CA3080 and CA 3080A High Performance Operational Transconductance Amplifiers”.

Pulse "droop" during the hold interval is 170pA/200pF which is 0.85µV/µs; (i.e., 170pA/200pF). In this case, 170pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000pF, the "hold-droop" rate will decrease to 0.085µV/µs, but the slew rate would decrease to 0.25V/µs. The parallel diode network connected between Terminal 3 of the CA3080A and Terminal 6 of the CA3140 prevents large input signal feedthrough across the input terminals of the CA3080A to the 200pF storage capacitor when the CA3080A is strobed off. Figure 24 shows dynamic characteristic waveforms of this sample-and-hold system.

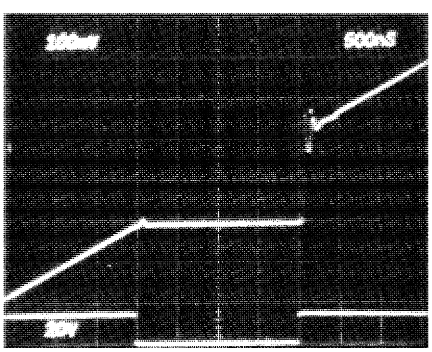


Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.



Top Trace: Output Signal; 5V/Div, 2µs/Div.
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div., 2µs/Div.
Bottom Trace: Input Signal; 5V/Div., 2µs/Div.

LARGE SIGNAL RESPONSE AND SETTLING TIME



SAMPLING RESPONSE

Top Trace: Output; 100mV/Div., 500ns/Div.
Bottom Trace: Input; 20V/Div., 500ns/Div.

FIGURE 24. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS

Current Amplifier

The low input terminal current needed to drive the CA3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 25 (see Note 14). In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R_2/R_1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100µA; a much easier current to measure in many systems.

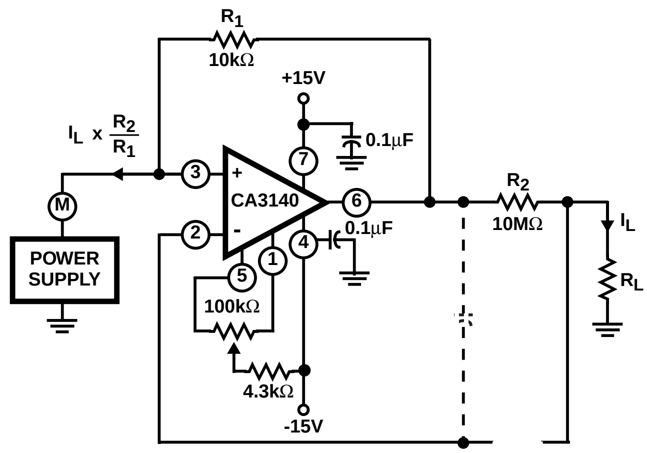


FIGURE 25. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

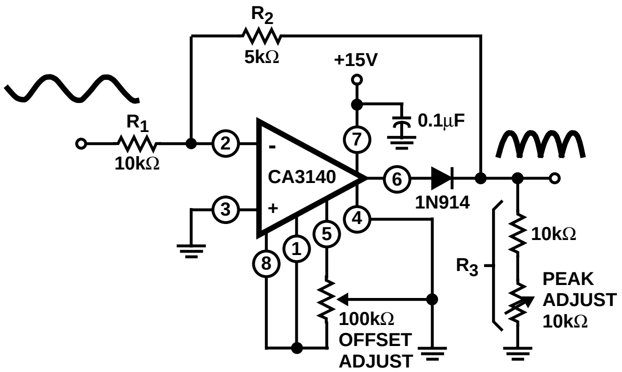
The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

Full Wave Rectifier

Figure 26 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 26 is satisfied, the full wave output is symmetrical.

NOTE:

14. "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308, "Negative Immittance Converter Circuits".



$$\text{GAIN} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 R_2 + R_3}$$

$$R_3 = \left(\frac{X + X^2}{1 - X}\right) R_1$$

$$\text{FOR } X = 0.5 \; \frac{5k\Omega}{10k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

$20V_{P-P}$ Input BW (-3dB) = 290kHz, DC Output (Avg) = 3.2V

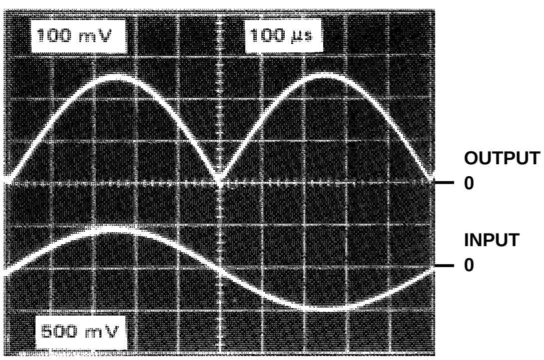


FIGURE 26. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

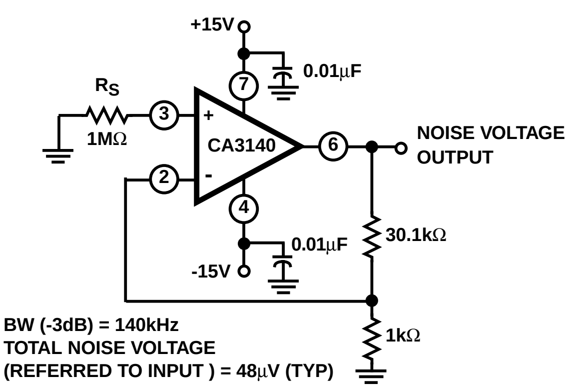


FIGURE 27. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

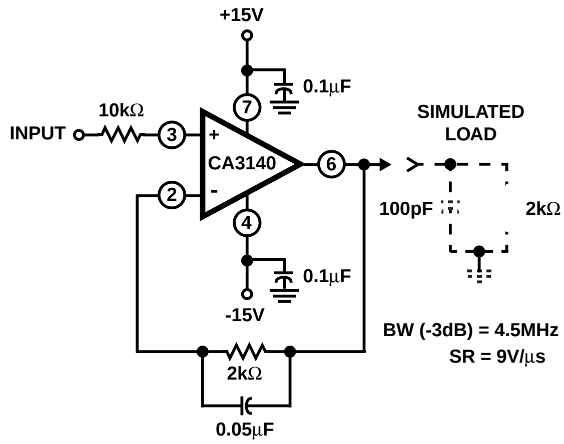
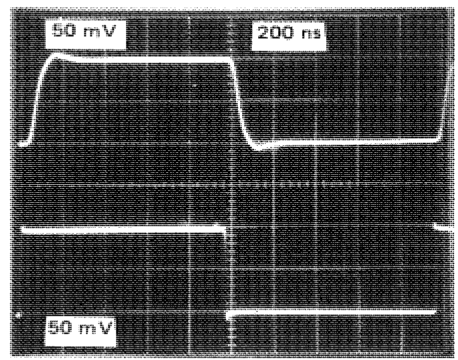


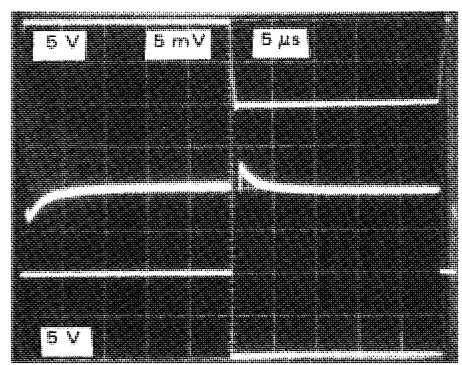
FIGURE 28A. TEST CIRCUIT



Top Trace: Output; 50mV/Div., 200ns/Div.

Bottom Trace: Input; 50mV/Div., 200ns/Div.

FIGURE 28B. SMALL SIGNAL RESPONSE



(Measurement made with Tektronix 7A13 differential amplifier.)

Top Trace: Output Signal; 5V/Div., 5μs/Div.

Center Trace: Difference Signal; 5mV/Div., 5μs/Div.

Bottom Trace: Input Signal; 5V/Div., 5μs/Div.

FIGURE 28C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 28. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves

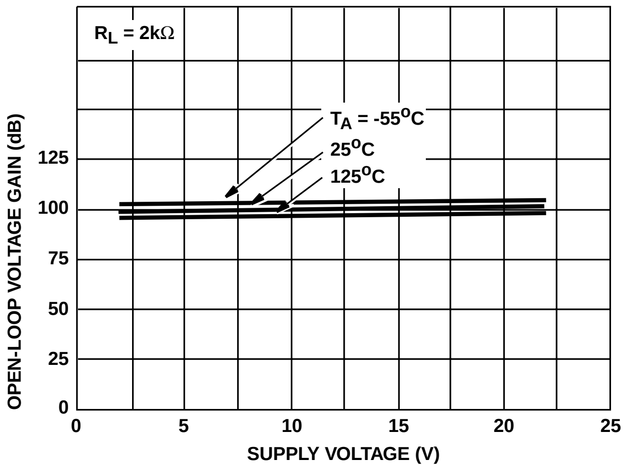


FIGURE 29. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

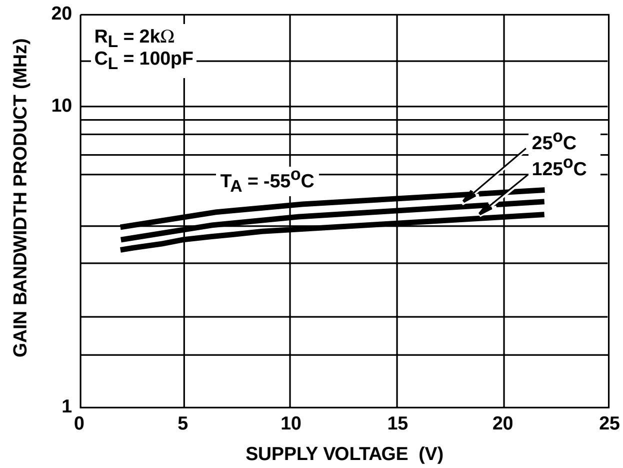


FIGURE 30. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

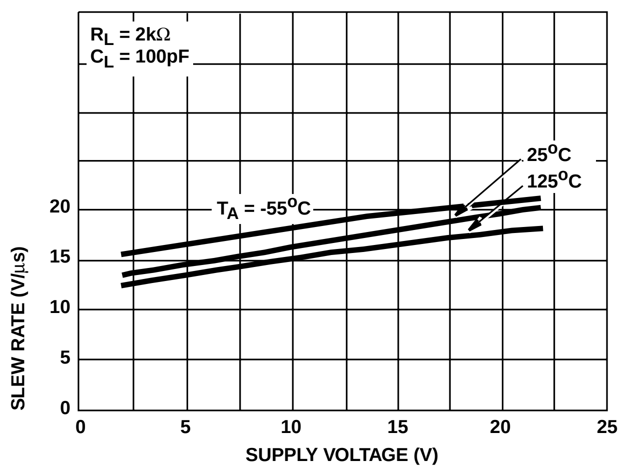


FIGURE 31. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

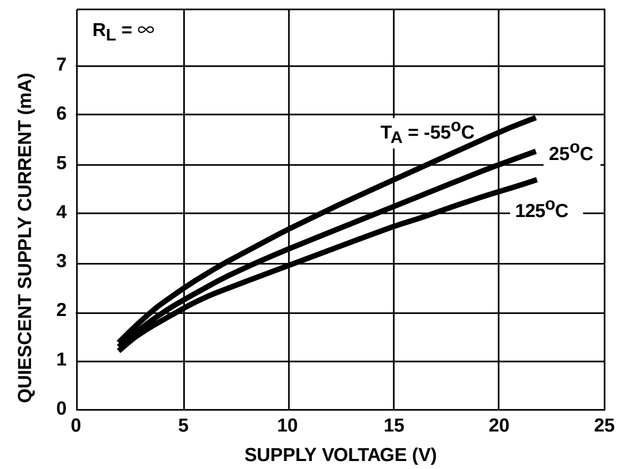


FIGURE 32. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

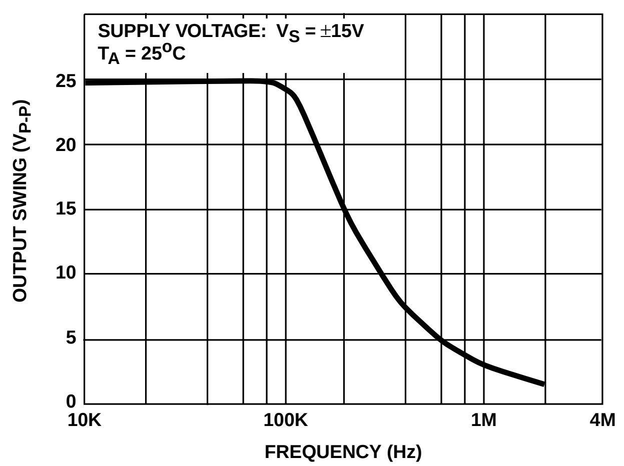


FIGURE 33. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

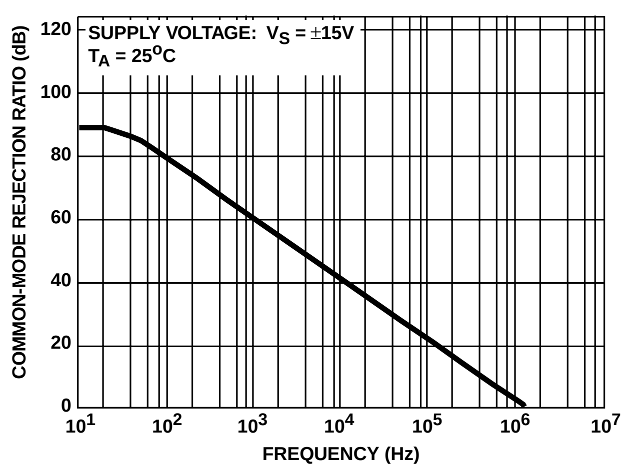


FIGURE 34. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

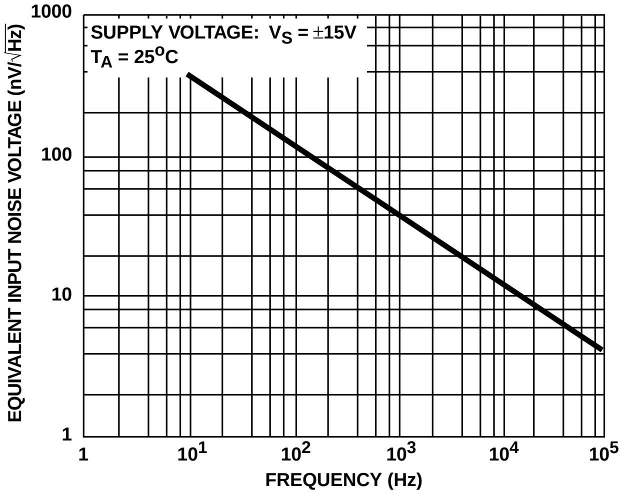


FIGURE 35. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

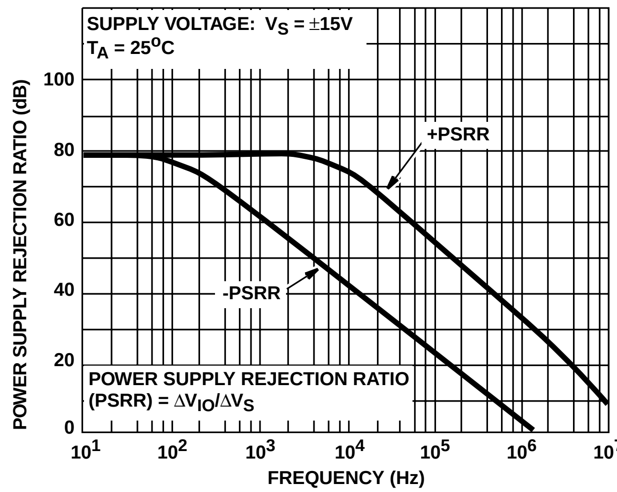
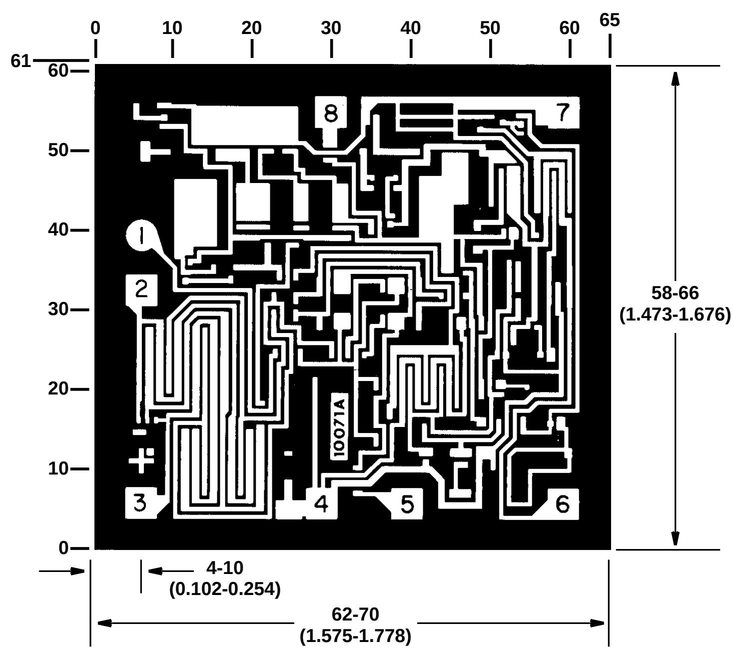


FIGURE 36. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

National Semiconductor

December 1995

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

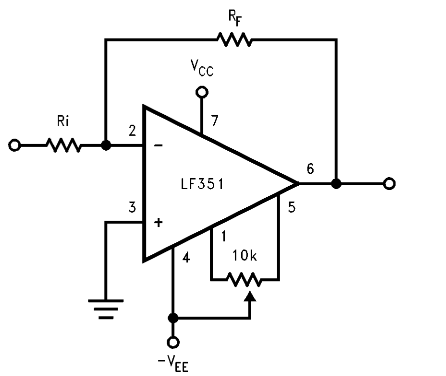
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

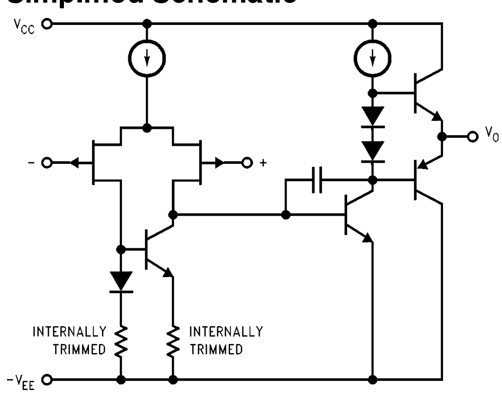
- Internally trimmed offset voltage — 10 mV
- Low input bias current — 50 pA
- Low input noise voltage — $25\ nV/\sqrt{Hz}$
- Low input noise current — $0.01\ pA/\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection



TL/H/5648–11

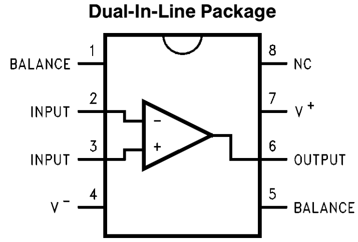
Simplified Schematic



TL/H/5648–12

Connection Diagrams

Dual-In-Line Package



TL/H/5648–13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C
θ_{jA}	
N Package	120°C/W
M Package	TBD
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ ±70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

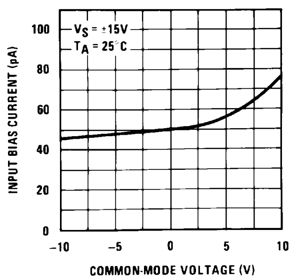
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

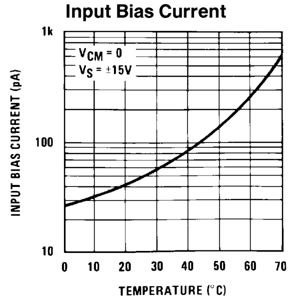
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

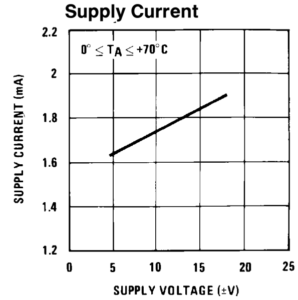
Input Bias Current



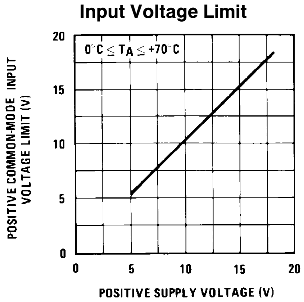
Input Bias Current



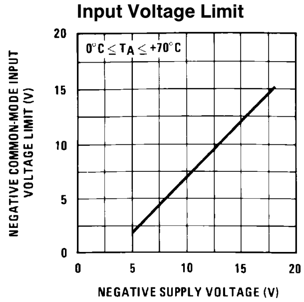
Supply Current



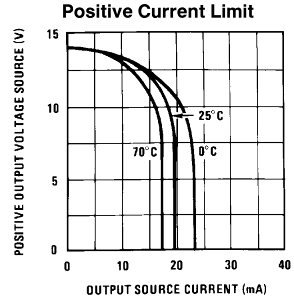
Positive Common-Mode Input Voltage Limit



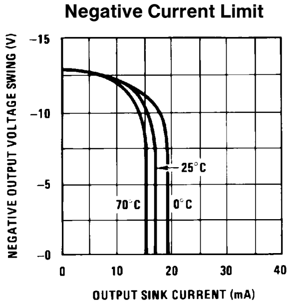
Negative Common-Mode Input Voltage Limit



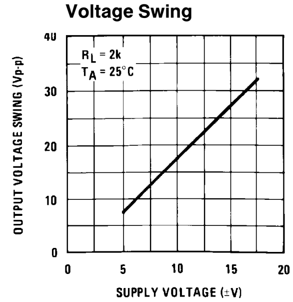
Positive Current Limit



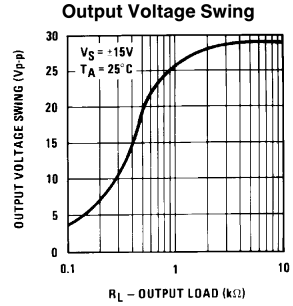
Negative Current Limit



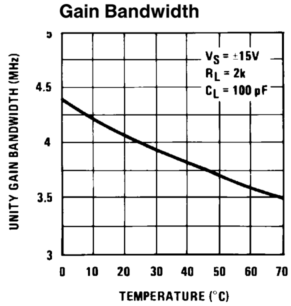
Voltage Swing



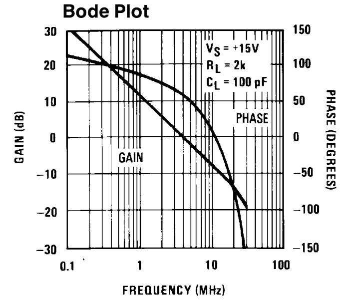
Output Voltage Swing



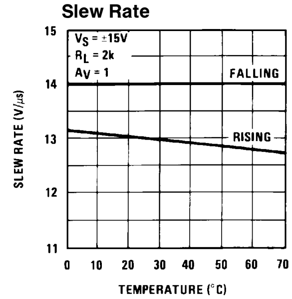
Gain Bandwidth



Bode Plot



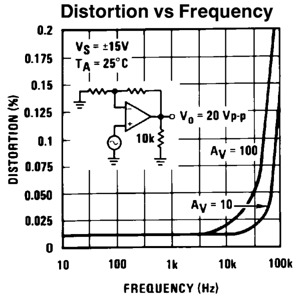
Slew Rate



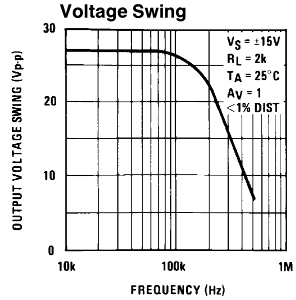
TL/H/5648–2

Typical Performance Characteristics (Continued)

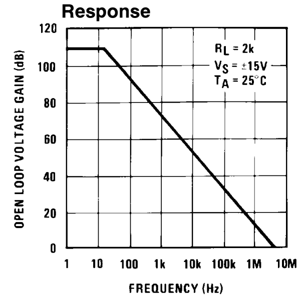
Distortion vs Frequency



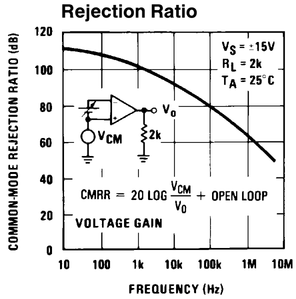
Undistorted Output Voltage Swing



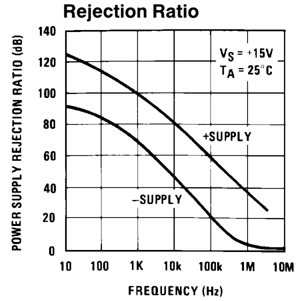
Open Loop Frequency Response



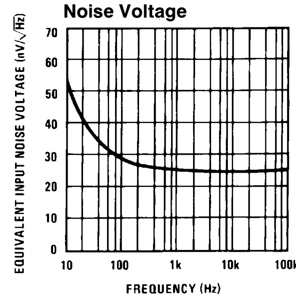
Common-Mode Rejection Ratio



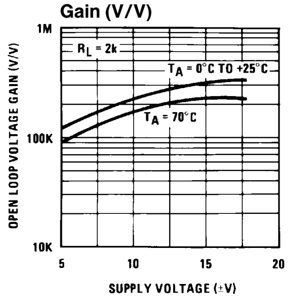
Power Supply Rejection Ratio



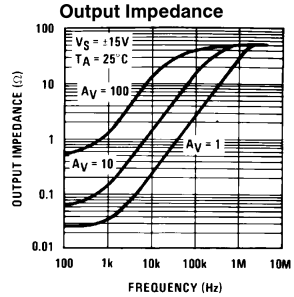
Equivalent Input Noise Voltage



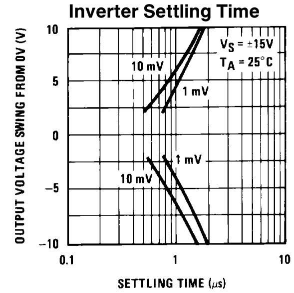
Open Loop Voltage Gain (V/V)



Output Impedance



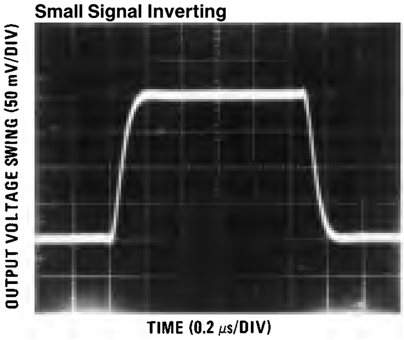
Inverter Settling Time



TL/H/5648–3

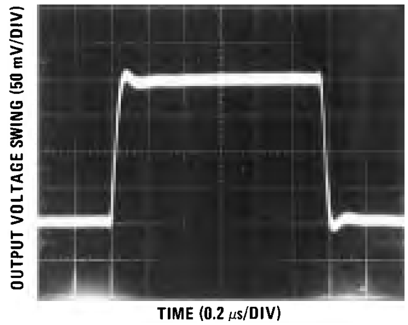
Pulse Response

Small Signal Inverting



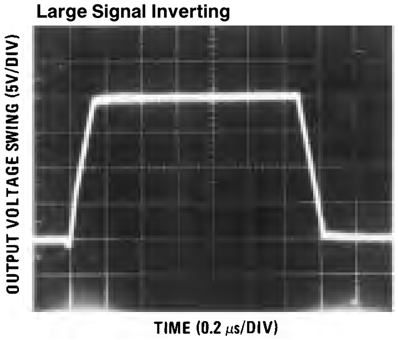
TL/H/5648–4

Small Signal Non-Inverting



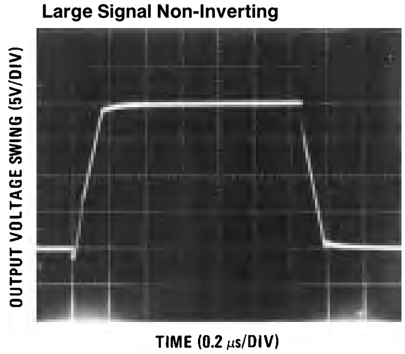
TL/H/5648–5

Large Signal Inverting



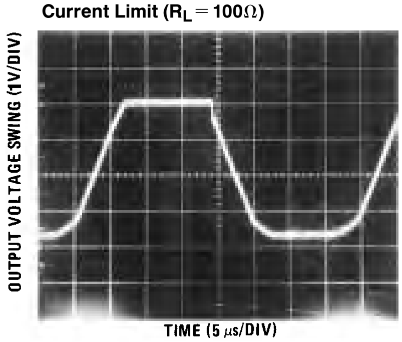
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit ($R_L = 100\Omega$)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

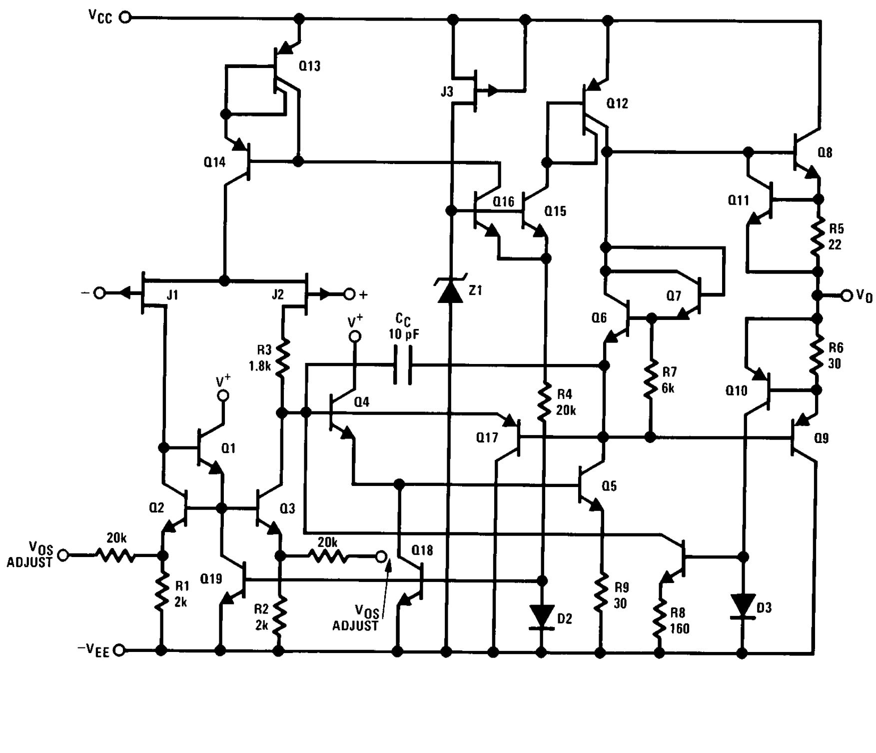
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

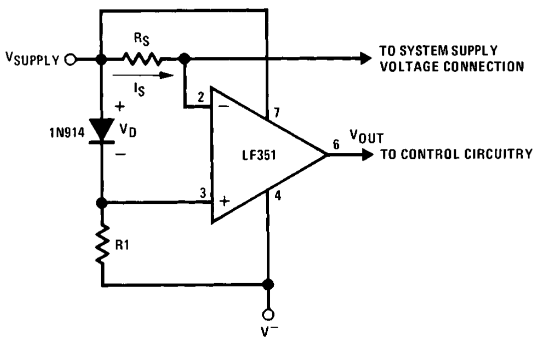
Detailed Schematic



TL/H/5648–9

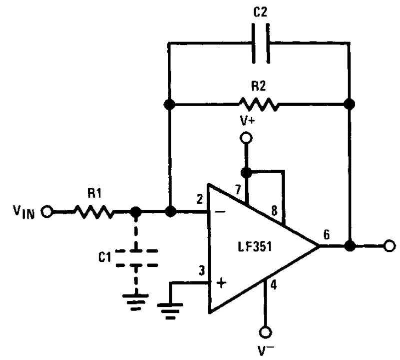
Typical Applications

Supply Current Indicator/Limiter



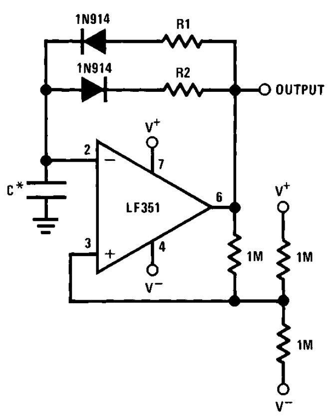
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 $\cong$ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 $\cong$ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

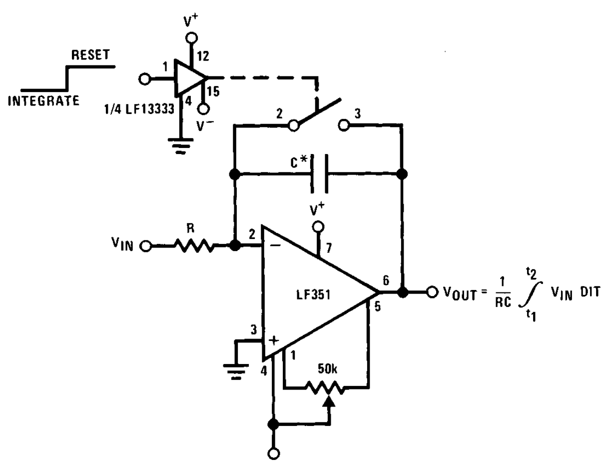


- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \dfrac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \dfrac{2V_S - 7.8}{V_S - 7.8}$

  where $V_S = V^+ + |V^-|$

  *low leakage capacitor

Long Time Integrator

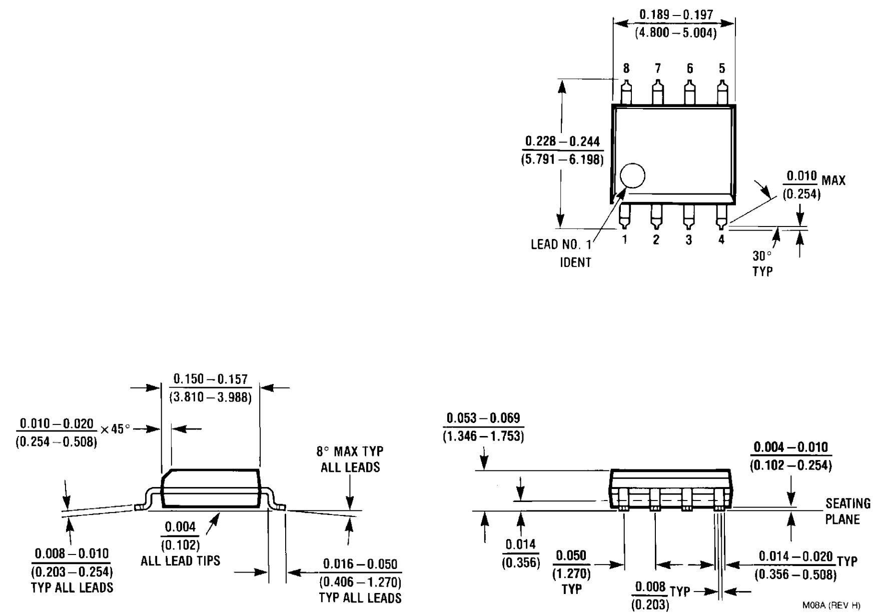


TL/H/5648–10

*Low leakage capacitor

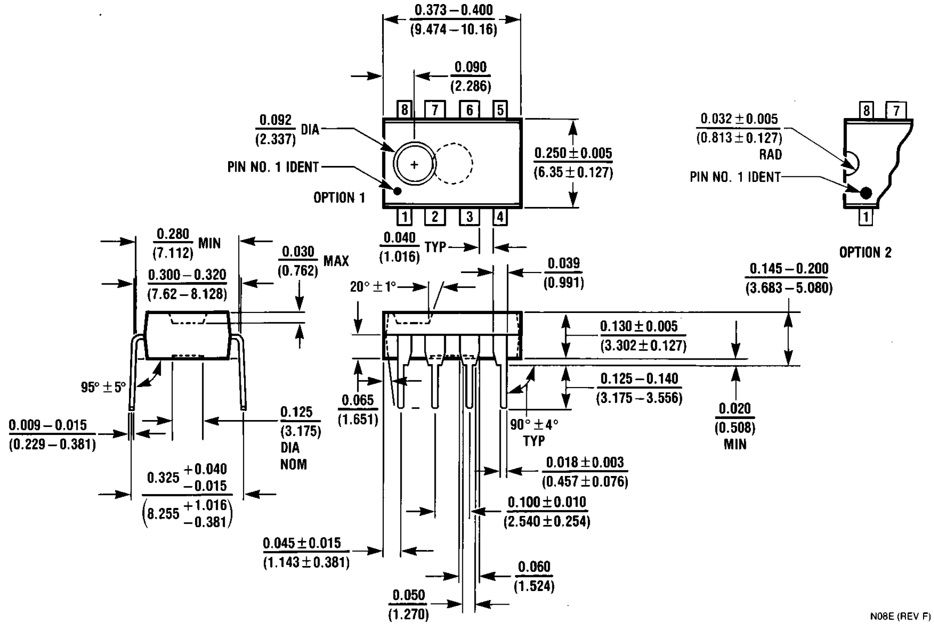
- 50k pot used for less sensitive V_{OS} adjust

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LF351M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF351N
NS Package Number N08E

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1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

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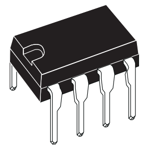
National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

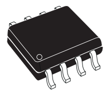
LM158,A-LM258,A
LM358,A

LOW POWER DUAL OPERATIONAL AMPLIFIERS

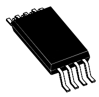
- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN : 100dB
- WIDE BANDWIDTH (unity gain) : 1.1MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/OP (500µA) - ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT : 20nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE : 2mV
- LOW INPUT OFFSET CURRENT : 2nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO (V_{CC} – 1.5V)



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)



P
TSSOP8
(Thin Shrink Small Outline Package)

DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

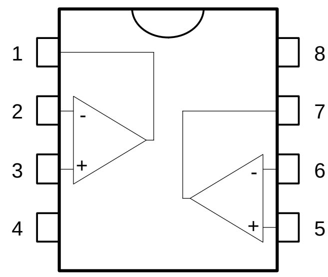
Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard + 5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

ORDER CODES

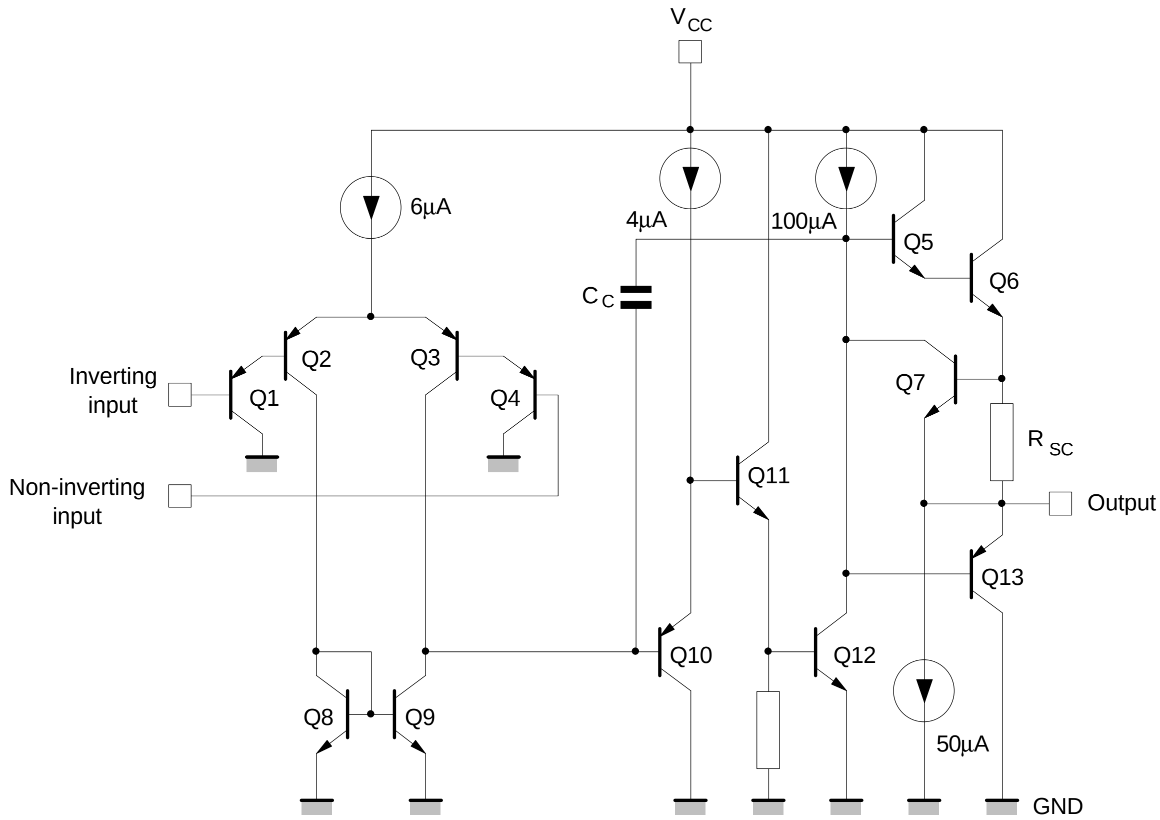
Part Number	Temperature Range	Package		
		N	D	P
LM158,A	–55°C, +125°C	•	•	•
LM258,A	–40°C, +105°C	•	•	•
LM358,A	0°C, +70°C	•	•	•
Example : LM258N				

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Ouput 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LM158)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V_{CC}	Supply Voltage	+32	+32	+32	V
V_i	Input Voltage	–0.3 to +32	–0.3 to +32	–0.3 to +32	V
V_{id}	Differential Input Voltage	+32	+32	+32	V
	Output Short-circuit Duration - (note 2)	Infinite			
P_{tot}	Power Dissipation	500	500	500	mW
I_{in}	Input Current - (note 1)	50	50	50	mA
T_{oper}	Operating Free-air Temperature Range	–55 to +125	–40 to +105	0 to +70	^{o}C
T_{stg}	Storage Temperature Range	–65 to +150	–65 to +150	–65 to +150	^{o}C

ELECTRICAL CHARACTERISTICS

V_{CC}^{+} = +5V, V_{CC}^{-} = Ground, V_O = 1.4V, T_{amb} = 25°C (unless otherwise specified)

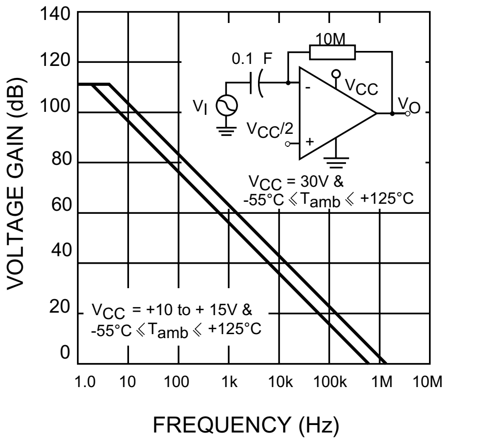
Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage - (note 3) T_{amb} = 25°C LM158, LM258 LM158A $T_{min.} \leq T_{amb} \leq T_{max.}$ LM158, LM258		1	3 2 4		2	7 5 9 7	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2	10 30		2	30 40	nA
I_{ib}	Input Bias Current - (note 4) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		20	50 100		20	150 200	nA
A_{vd}	Large Signal Voltage Gain (V_{CC} = +15V, R_L = 2kΩ, V_O = 1.4V to 11.4V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	100		50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 10kΩ) (V_{CC}^{+} = 5 to 30V) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	65 65	100		65 65	100		dB
I_{CC}	Supply Current, all Amp, no Load V_{CC} = +5V, $T_{min.} \leq T_{amb} \leq T_{max.}$ V_{CC} = +30V, $T_{min.} \leq T_{amb} \leq T_{max.}$		0.7	1.2 2		0.7	1.2 2	mA
V_{icm}	Input Common Mode Voltage Range (V_{CC} = +30V) - (note 6) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0 0		V_{CC}^{+}–1.5 V_{CC}^{+}–2	0 0		V_{CC}^{+}–1.5 V_{CC}^{+}–2	V
CMR	Common-mode Rejection Ratio (R_S = 10kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	70 60	85		70 60	85		dB
I_{source}	Output Current Source (V_{CC} = +15V, V_o = 2V, V_{id} = +1V)	20	40	60	20	40	60	mA
I_{sink}	Output Current Sink (V_{id} = -1V) V_{CC} = +15V, V_O = 2V V_{CC} = +15V, V_O = +0.2V	10 12	20 50		10 12	20 50		mA µA
V_{OPP}	Output Voltage Swing (R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0 0		V_{CC}^{+}–1.5 V_{CC}^{+}–2	0 0		V_{CC}^{+}–1.5 V_{CC}^{+}–2	V
V_{OH}	High Level Output Voltage (V_{CC}^{+} = 30V) T_{amb} = 25°C R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ T_{amb} = 25°C R_L = 10kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$	26 26 27 27	27 28		26 26 27 27	27 28		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 20		5	20 20	mV
SR	Slew Rate (V_{CC} = 15V, V_I = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity gain)	0.3	0.6		0.3	0.6		V/µs
GBP	Gain Bandwidth Product (V_{CC} = 30V, f = 100kHz, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF)	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_{CC} = 30V, C_L = 100pF, V_O = 2 $_{PP}$)		0.02			0.02		%
e_n	Equivalent Input Noise voltage (f = 1kHz, R_s = 100Ω, V_{CC} = 30V)		55			55		$\frac{nV}{\sqrt{Hz}}$

ELECTRICAL CHARACTERISTICS (continued)

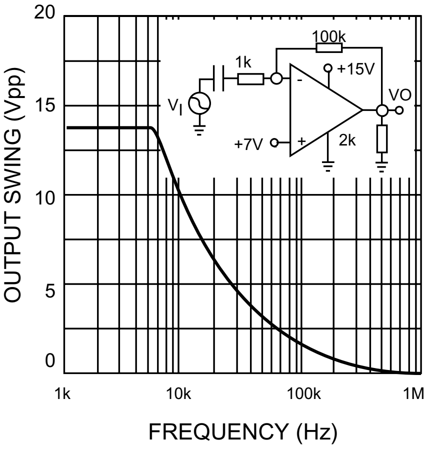
Symbol	Parameter	LM158A LM258A LM358A			LM158 LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DV_{io}	Input Offset Voltage Drift		7	15		7	30	μV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{O1}/V_{O2}	Channel Separation (note 5) $1kHz \leq f \leq 20kHz$		120			120		dB

Notes :
1. This input current only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than –0.3V.
2. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC}^+ > 15V$. The maximum output current is approximatively 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. $V_O = 1.4V$, $R_S = 0\Omega$, $5V < V_{CC}^+ < 30V$, $0 < V_{ic} < V_{CC}^+ - 1.5V$.
4. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
5. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.
6. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$. But either or both inputs can go to +32V without damage.

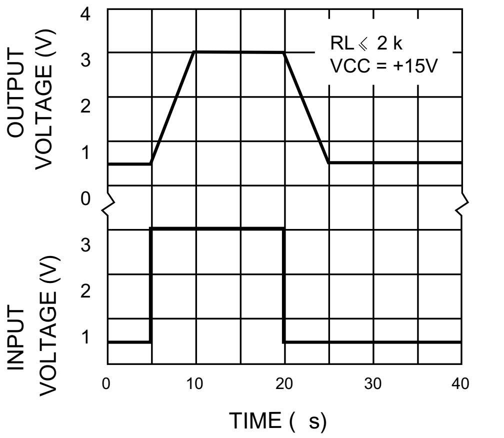
OPEN LOOP FREQUENCY RESPONSE (NOTE 3)



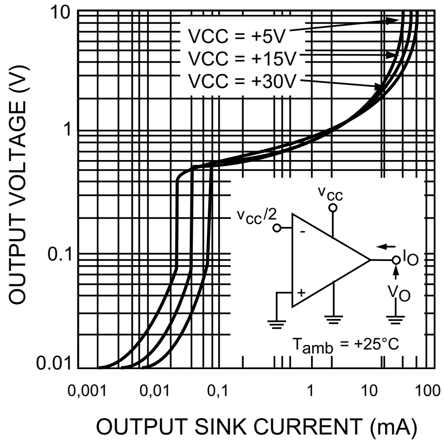
LARGE SIGNAL FREQUENCY RESPONSE



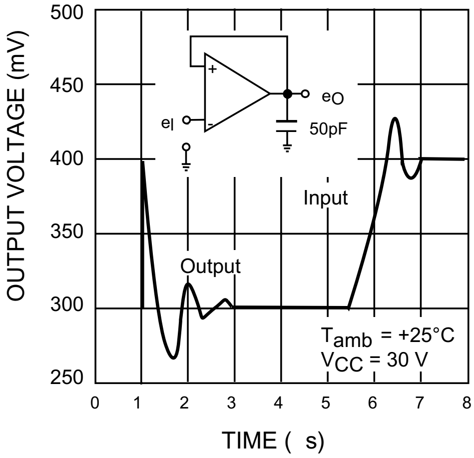
VOLAGE FOLLOWER PULSE RESPONSE



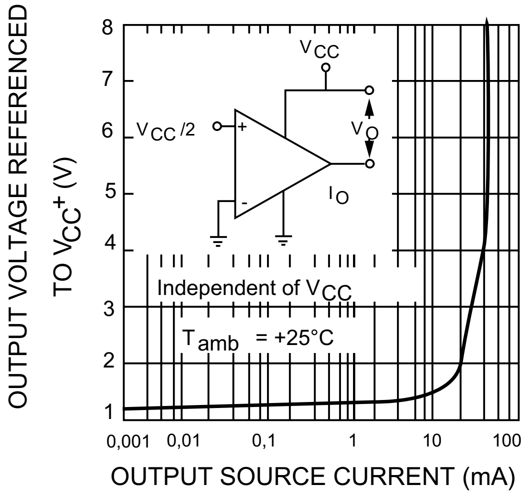
OUTPUT CHARACTERISTICS



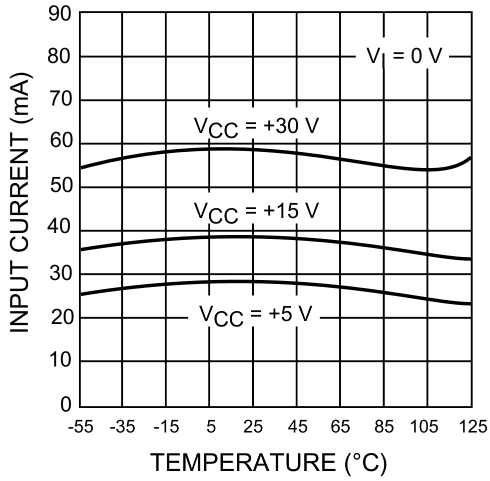
VOLTAGE FOLLOWER PULSSE RESPONSE
(SMALL SIGNAL)



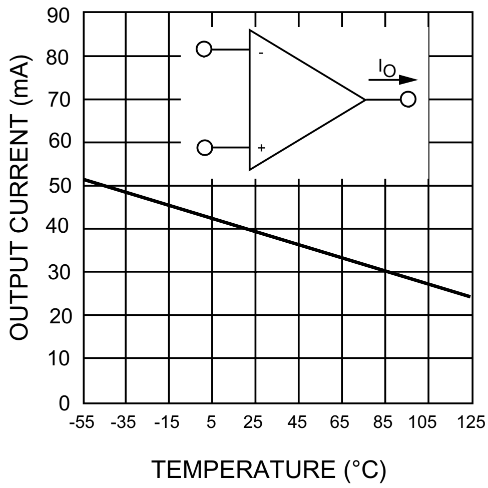
OUTPUT CHARACTERISTICS



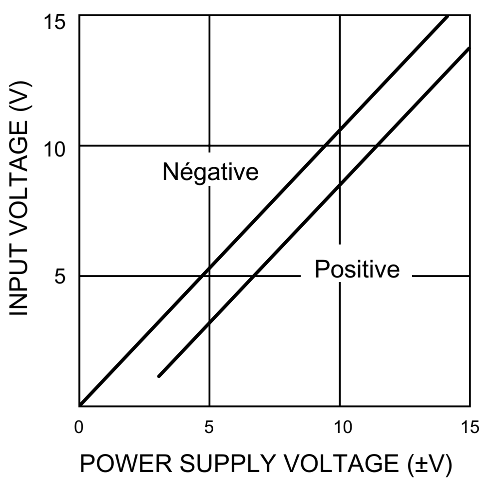
INPUT CURRENT (Note 1)



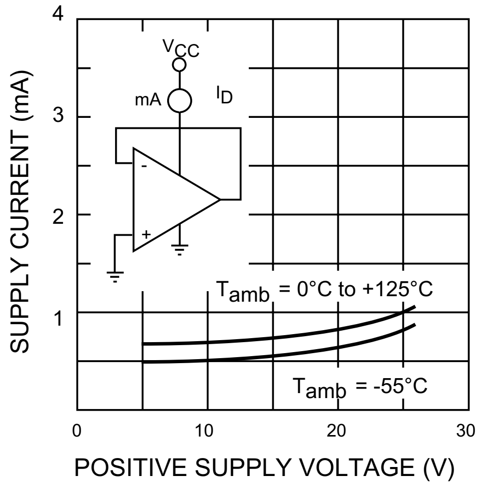
CURRENT LIMITING (Note 1)

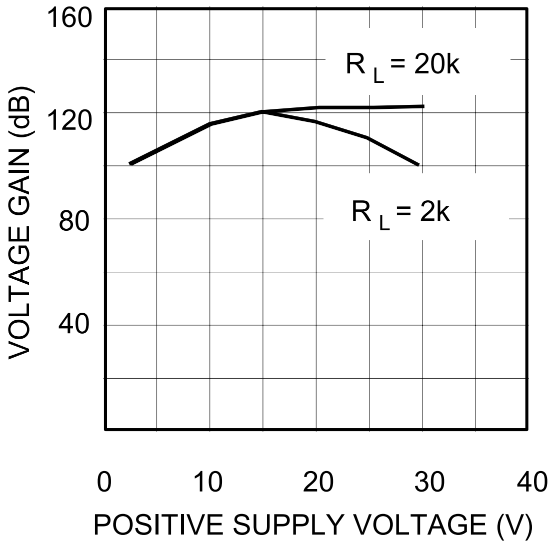


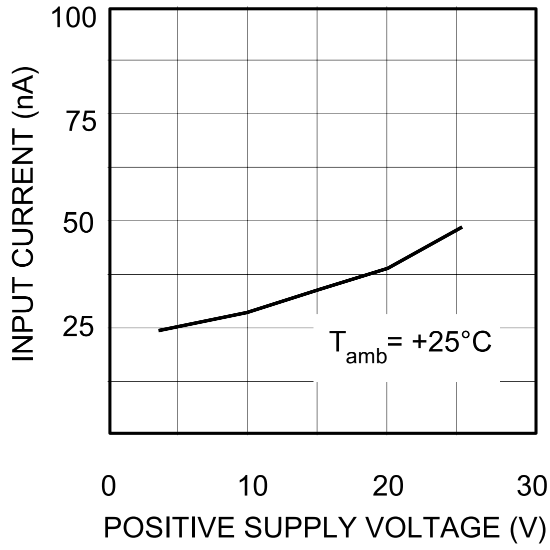
INPUT VOLTAGE RANGE

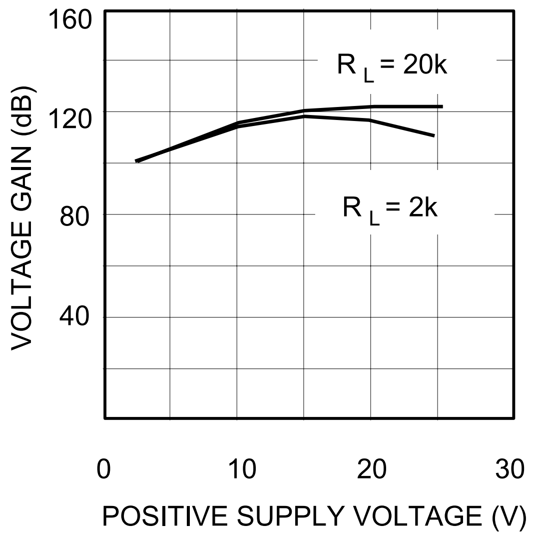


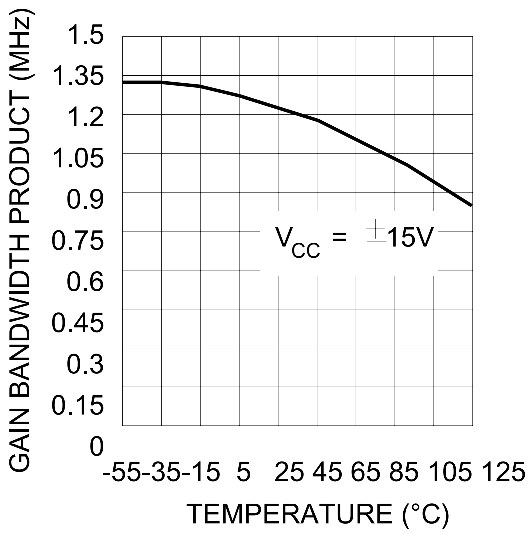
SUPPLY CURRENT

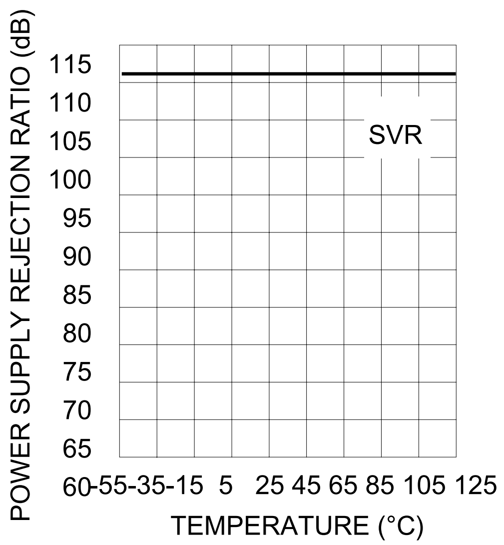


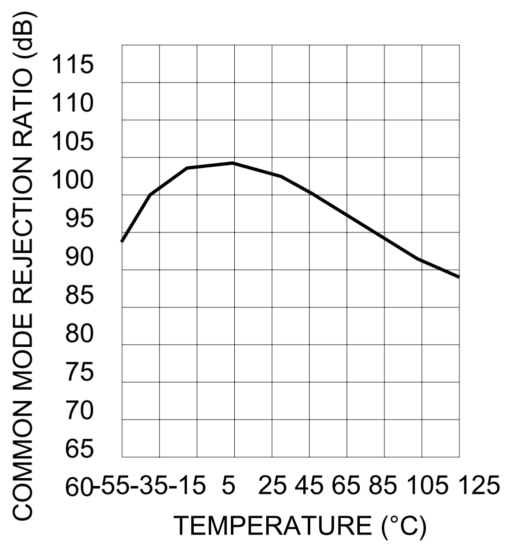

160
120
80
40
VOLTAGE GAIN (dB)
R L = 20k
R L = 2k
0 10 20 30 40
POSITIVE SUPPLY VOLTAGE (V)


100
75
50
25
INPUT CURRENT (nA)
Tamb= +25°C
0 10 20 30
POSITIVE SUPPLY VOLTAGE (V)


160
120
80
40
VOLTAGE GAIN (dB)
R L = 20k
R L = 2k
0 10 20 30
POSITIVE SUPPLY VOLTAGE (V)

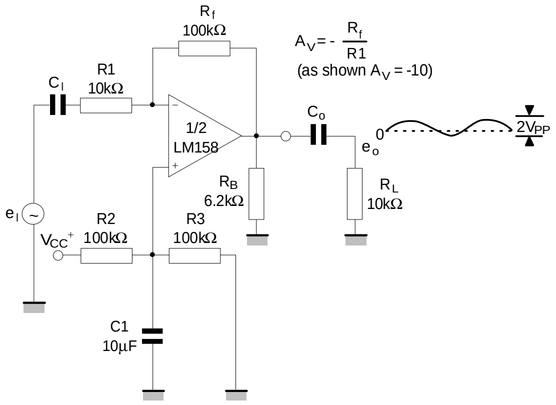

1.5
1.35
1.2
1.05
0.9
0.75
0.6
0.45
0.3
0.15
0
GAIN BANDWIDTH PRODUCT (MHz)
VCC = ±15V
-55-35-15 5 25 45 65 85 105 125
TEMPERATURE (°C)


115
110
105
100
95
90
85
80
75
70
65
60
POWER SUPPLY REJECTION RATIO (dB)
SVR
-55-35-15 5 25 45 65 85 105 125
TEMPERATURE (°C)

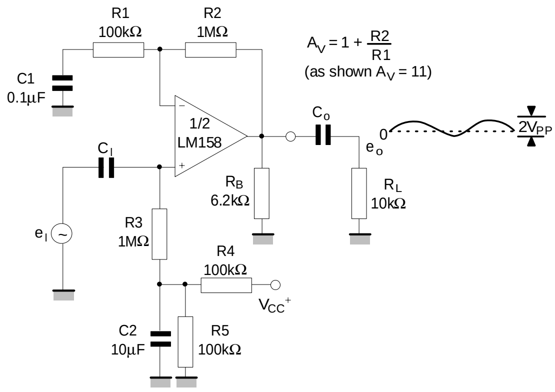

115
110
105
100
95
90
85
80
75
70
65
60
COMMON MODE REJECTION RATIO (dB)
-55-35-15 5 25 45 65 85 105 125
TEMPERATURE (°C)

TYPICAL APPLICATIONS (single supply voltage) $V_{CC} = +5V_{DC}$

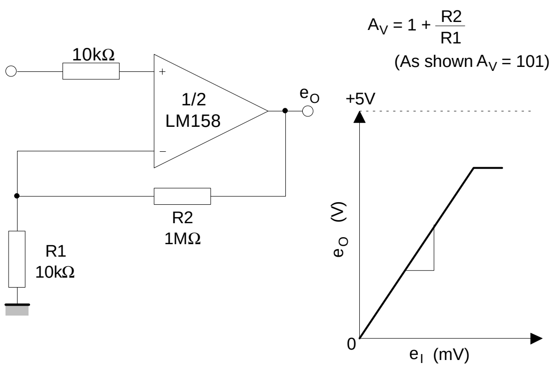
AC COUPLED INVERTING AMPLIFIER



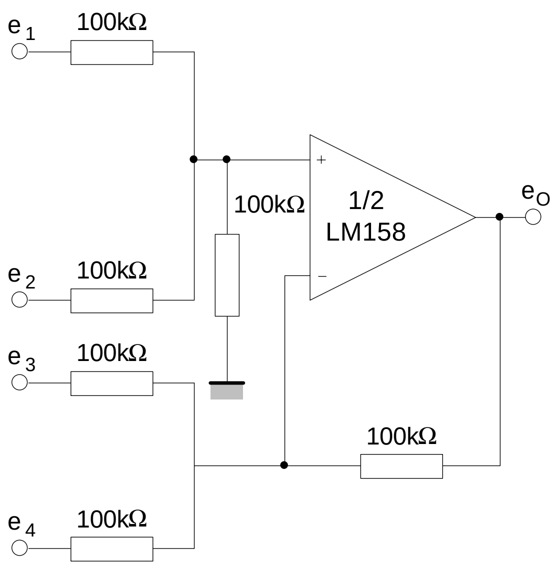
AC COUPLED NON-INVERTING AMPLIFIER



NON-INVERTING DC AMPLIFIER

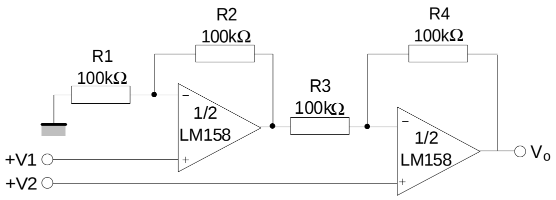


DC SUMMING AMPLIFIER



$e_o = e_1 + e_2 - e_3 - e_4$
where $(e_1 + e_2) \geq (e_3 + e_4)$
to keep $e_o \geq 0V$

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

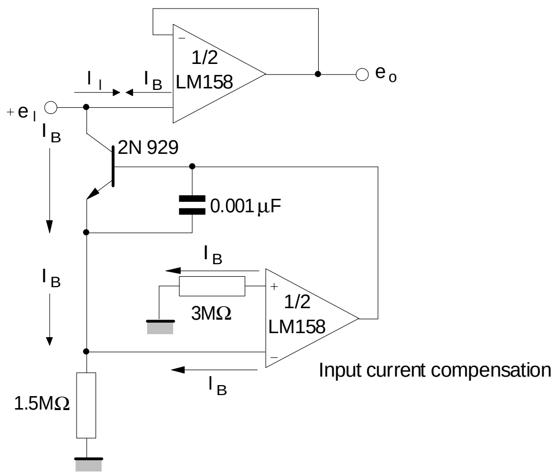


if $R_1 = R_5$ and $R_3 = R_4 = R_6 = R_7$

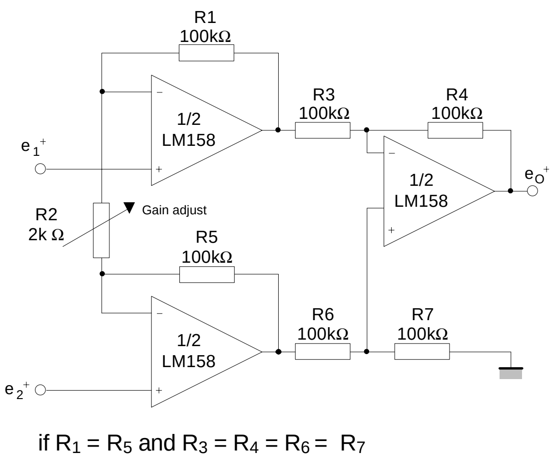
$$e_o = [\,1+\frac{2R_1}{R_2}\,]\,(e_2 - e_1)$$

As shown $e_o = 101\ (e_2 - e_1)$.

USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT



HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

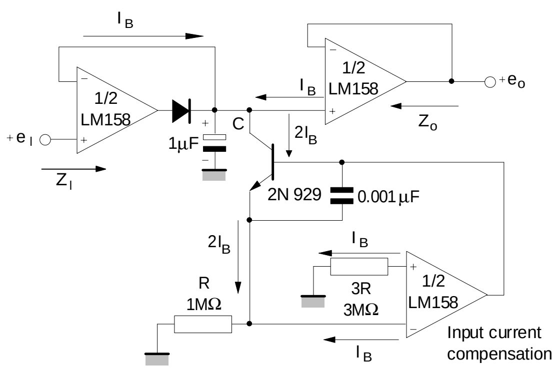


if $R_1 = R_5$ and $R_3 = R_4 = R_6 = R_7$

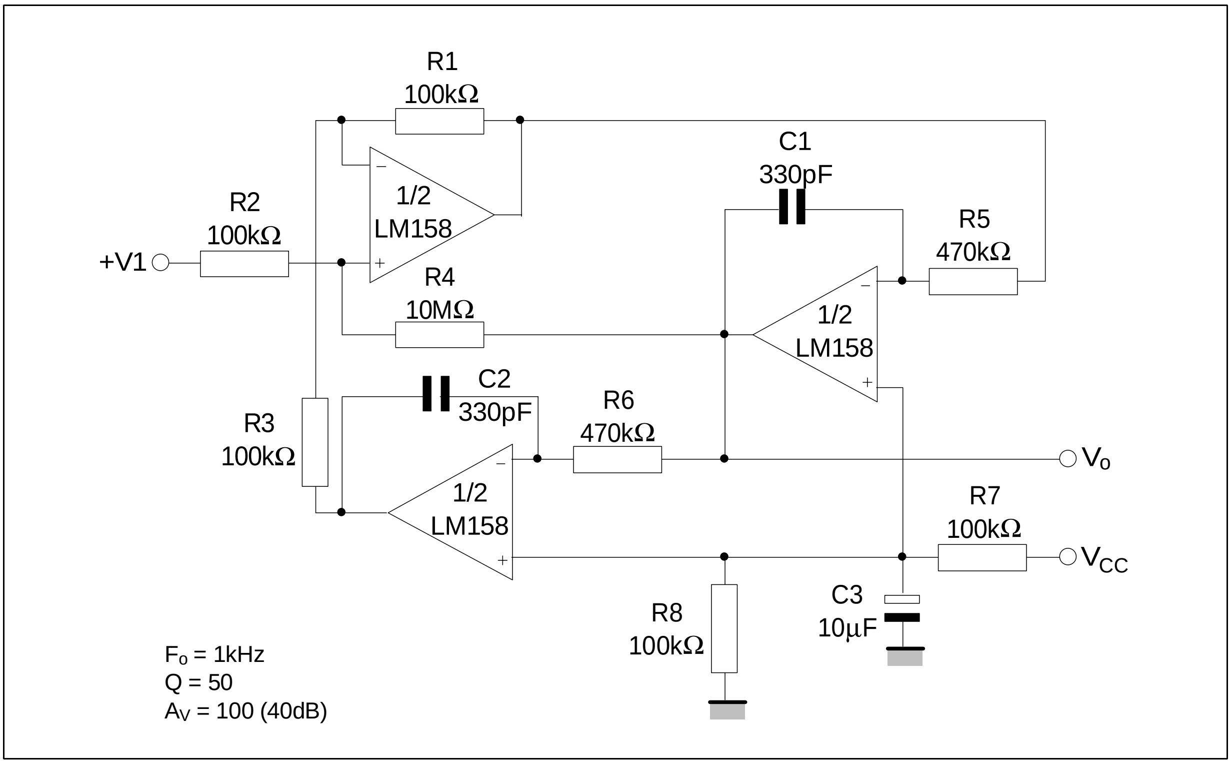
$$e_o = [\,1+\frac{2R_1}{R_2}\,]\,(e_2 - e_1)$$

As shown $e_o = 101\ (e_2 - e_1)$

LOW DRIFT PEAK DETECTOR

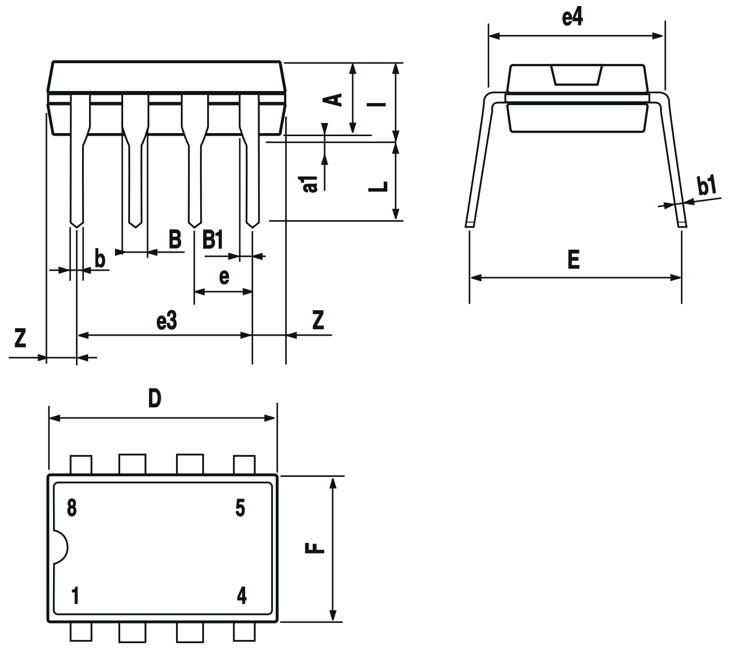


ACTIVE BAND-PASS FILTER



PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



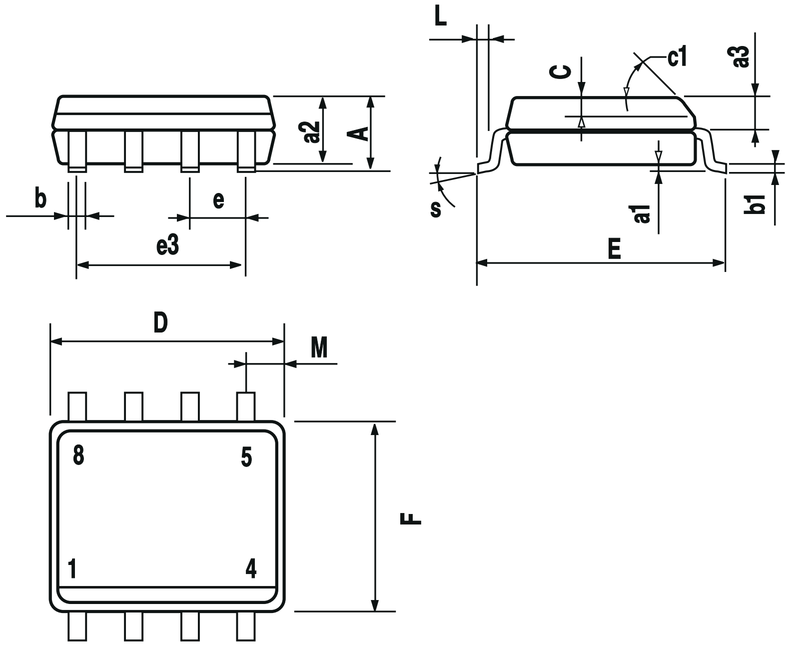
PM-DIP8.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)

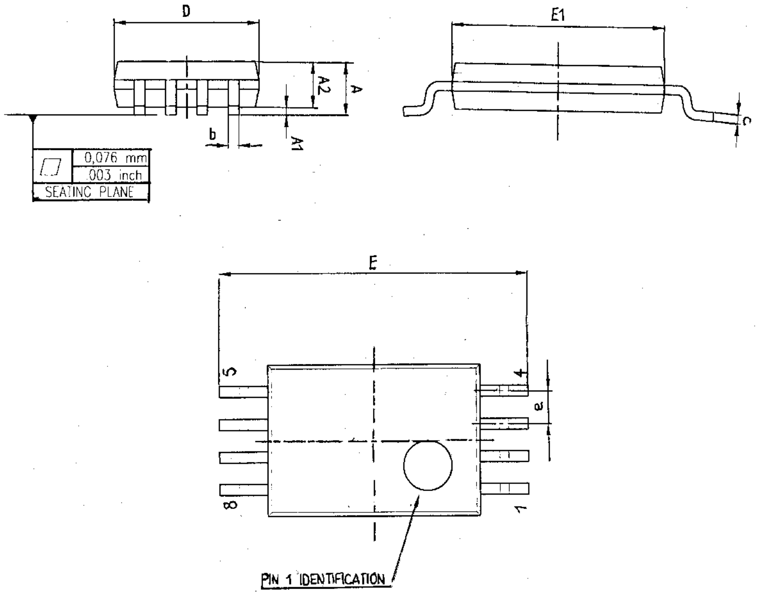


PM-SO8.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45^{o} (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8^{o} (max.)					

SO8.TBL

PACKAGE MECHANICAL DATA
8 PINS - THIN SHRINK SMALL OUTLINE PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0^o		8^o	0^o		8^o
l	0.50	0.60	0.75	0.09	0.0236	0.030

Ultralow Offset Voltage Operational Amplifier

Data Sheet

OP07

FEATURES

Low V_{OS}: 75 μV maximum
Low V_{OS} drift: 1.3 μV/°C maximum
Ultrastable vs. time: 1.5 μV per month maximum
Low noise: 0.6 μV p-p maximum
Wide input voltage range: ±14 V typical
Wide supply voltage range: ±3 V to ±18 V
125°C temperature-tested dice

APPLICATIONS

Wireless base station control circuits
Optical network control circuits
Instrumentation
Sensors and controls
- **Thermocouples**
- **Resistor thermal detectors (RTDs)**
- **Strain bridges**
- **Shunt current measurements**

Precision filters

GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75 μV maximum for OP07E) that is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (±4 nA for the OP07E) and high open-loop gain (200 V/mV for the OP07E). The low offset and high open-loop gain make the OP07 particularly useful for high gain instrumentation applications.

PIN CONFIGURATION

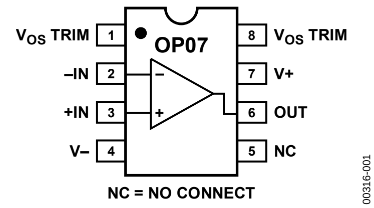


Figure 1.

The wide input voltage range of ±13 V minimum combined with a high CMRR of 106 dB (OP07E) and high input impedance provide high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications.

The OP07 is available in two standard performance grades. The OP07E is specified for operation over the 0°C to 70°C range, and the OP07C is specified over the −40°C to +85°C temperature range.

The OP07 is available in epoxy 8-lead PDIP and 8-lead narrow SOIC packages. For CERDIP and TO-99 packages and standard microcircuit drawing (SMD) versions, see the OP77.

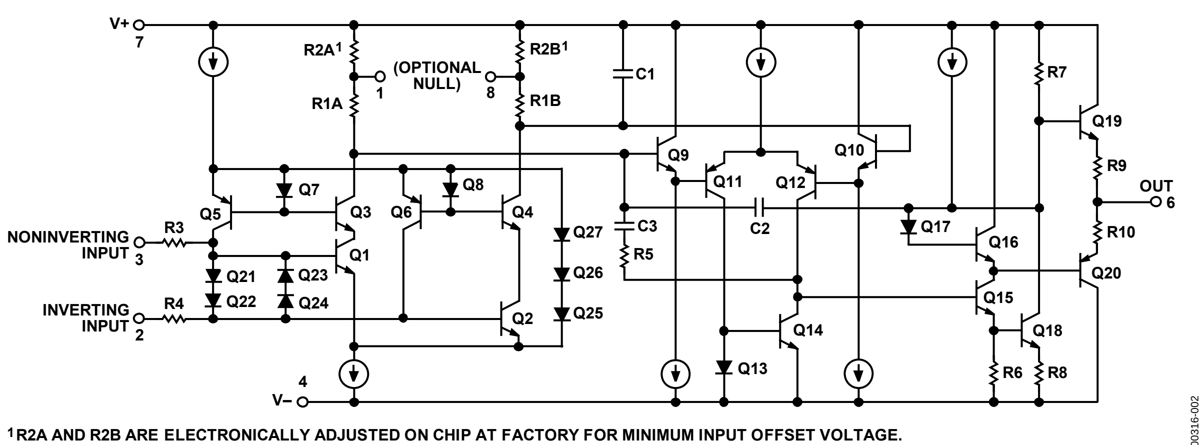


Figure 2. Simplified Schematic

Rev. G

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SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS

V_S = ±15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
T_A = 25°C						
Input Offset Voltage[1]	V_{OS}			30	75	µV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.3	1.5	µV/Month
Input Offset Current	I_{OS}			0.5	3.8	nA
Input Bias Current	I_B			±1.2	±4.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		10.3	18.0	nV/√Hz
		f_O = 100 Hz[3]		10.0	13.0	nV/√Hz
		f_O = 1 kHz		9.6	11.0	nV/√Hz
Input Noise Current	I_n p-p			14	30	pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		0.32	0.80	pA/√Hz
		f_O = 100 Hz[3]		0.14	0.23	pA/√Hz
		f_O = 1 kHz		0.12	0.17	pA/√Hz
Input Resistance, Differential Mode[4]	R_{IN}		15	50		MΩ
Input Resistance, Common Mode	R_{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		5	20	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	200	500		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	150	400		V/mV
0°C ≤ T_A ≤ 70°C						
Input Offset Voltage[1]	V_{OS}			45	130	µV
Voltage Drift Without External Trim[4]	TCV_{OS}			0.3	1.3	µV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P = 20 kΩ		0.3	1.3	µV/°C
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	pA/°C
Input Bias Current	I_B			±1.5	±5.5	nA
Input Bias Current Drift	TCI_B			13	35	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	103	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		7	32	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	180	450		V/mV
OUTPUT CHARACTERISTICS						
T_A = 25°C						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.5	±13.0		V
		R_L ≥ 2 kΩ	±12.0	±12.8		V
		R_L ≥ 1 kΩ	±10.5	±12.0		V
0°C ≤ T_A ≤ 70°C						
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±12.6		V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	R_L ≥ 2 kΩ[3]	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A_{VOL} = 1[5]	0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60		Ω
Power Consumption	P_d	V_S = ±15 V, No load		75	120	mW
		V_S = ±3 V, No load		4	6	mW
Offset Adjustment Range		R_P = 20 kΩ		±4		mV

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2] Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.
[3] Sample tested.
[4] Guaranteed by design.
[5] Guaranteed but not tested.

OP07C ELECTRICAL CHARACTERISTICS

V_S = ±15 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
T_A = 25°C						
Input Offset Voltage[1]	V_{OS}			60	150	μV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.4	2.0	μV/Month
Input Offset Current	I_{OS}			0.8	6.0	nA
Input Bias Current	I_B			±1.8	±7.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.38	0.65	μV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		10.5	20.0	nV/√Hz
		f_O = 100 Hz[3]		10.2	13.5	nV/√Hz
		f_O = 1 kHz		9.8	11.5	nV/√Hz
Input Noise Current	I_n p-p			15	35	pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		0.35	0.90	pA/√Hz
		f_O = 100 Hz[3]		0.15	0.27	pA/√Hz
		f_O = 1 kHz		0.13	0.18	pA/√Hz
Input Resistance, Differential Mode[4]	R_{IN}		8	33		MΩ
Input Resistance, Common Mode	R_{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		7	32	μV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	120	400		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	100	400		V/mV
−40°C ≤ T_A ≤ +85°C						
Input Offset Voltage[1]	V_{OS}			85	250	μV
Voltage Drift Without External Trim[4]	TCV_{OS}			0.5	1.8	μV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P = 20 kΩ		0.4	1.6	μV/°C
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI_{OS}			12	50	pA/°C
Input Bias Current	I_B			±2.2	±9.0	nA
Input Bias Current Drift	TCI_B			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	97	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		10	51	μV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	100	400		V/mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
T_A = 25°C						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.0	±13.0		V
		R_L ≥ 2 kΩ	±11.5	±12.8		V
		R_L ≥ 1 kΩ		±12.0		V
−40°C ≤ T_A ≤ +85°C						
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±12.6		V
DYNAMIC PERFORMANCE						
T_A = 25°C						
Slew Rate	SR	R_L ≥ 2 kΩ[3]	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	A_{VOL} = 1 [5]	0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60		Ω
Power Consumption	P_d	V_S = ±15 V, No load		80	150	mW
		V_S = ±3 V, No load		4	8	mW
Offset Adjustment Range		R_P = 20 kΩ		±4		mV

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2] Long-term input offset voltage stability refers to the averaged trend time of V_{OS} vs. the time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Refer to the Typical Performance Characteristics section. Parameter is sample tested.
[3] Sample tested.
[4] Guaranteed by design.
[5] Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage (V_S)	±22 V
Input Voltage[1]	±22 V
Differential Input Voltage	±30 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
S and P Packages	−65°C to +125°C
Operating Temperature Range	
OP07E	0°C to 70°C
OP07C	−40°C to +85°C
Junction Temperature	150°C
Lead Temperature, Soldering (60 sec)	300°C

[1] For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC_N (S-Suffix)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

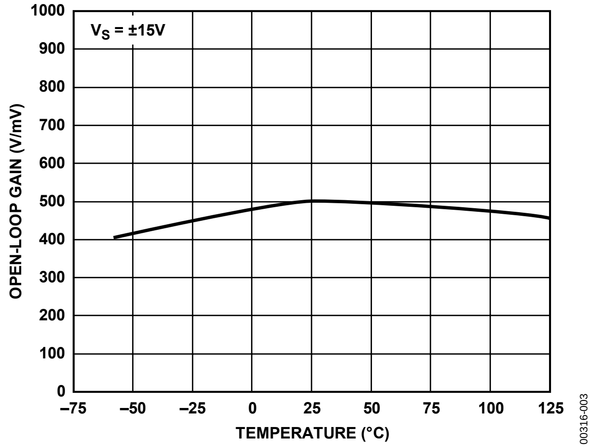


Figure 3. Open-Loop Gain vs. Temperature

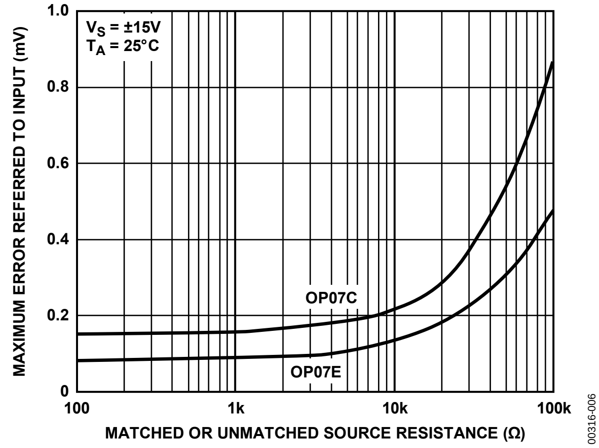


Figure 6. Maximum Error vs. Source Resistance

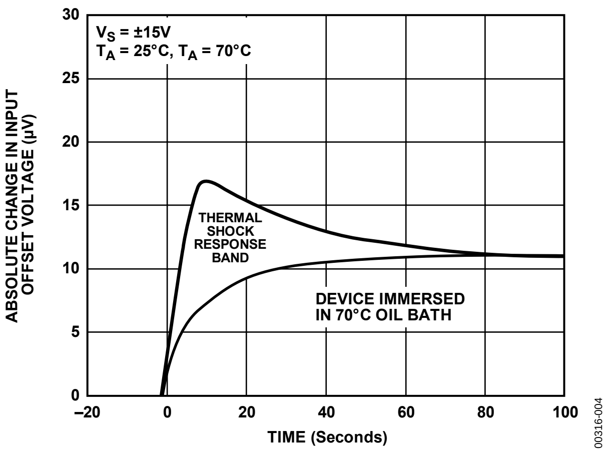


Figure 4. Offset Voltage Change due to Thermal Shock

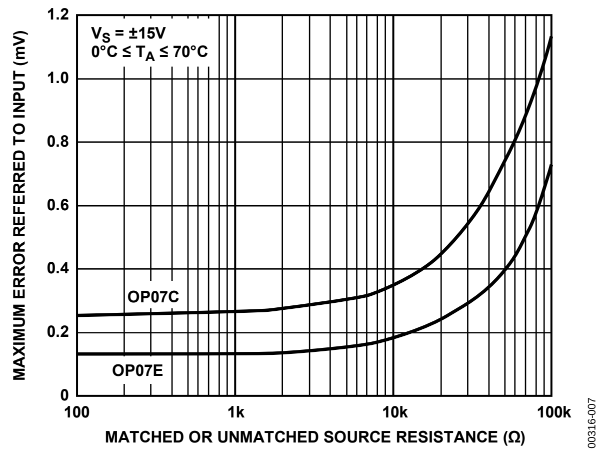


Figure 7. Maximum Error vs. Source Resistance

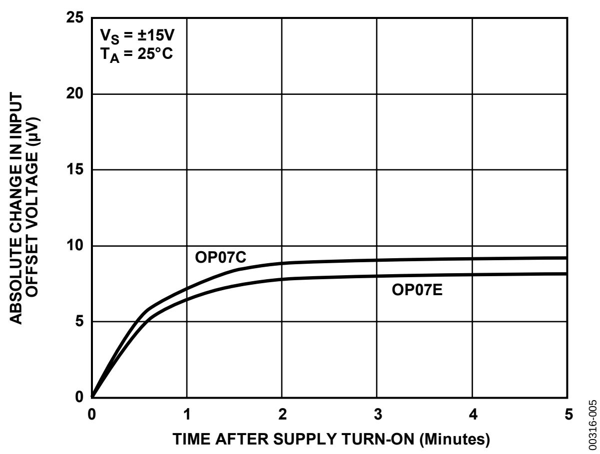


Figure 5. Warm-Up Drift

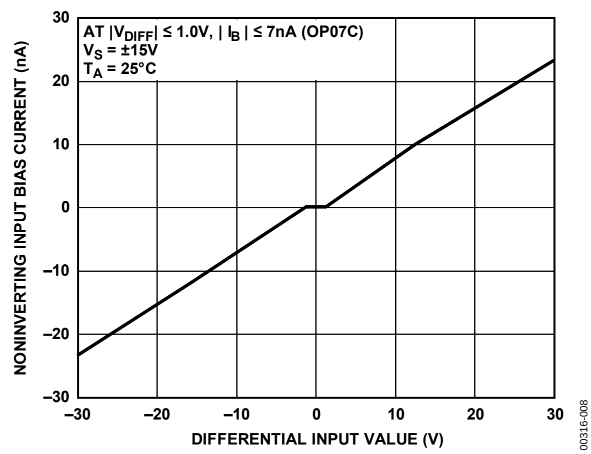


Figure 8. Input Bias Current vs. Differential Input Voltage

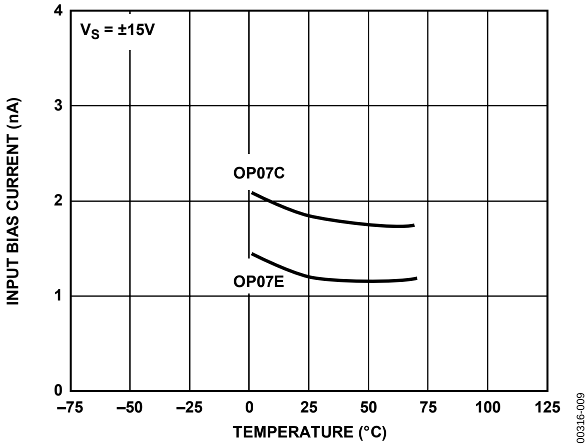


Figure 9. Input Bias Current vs. Temperature

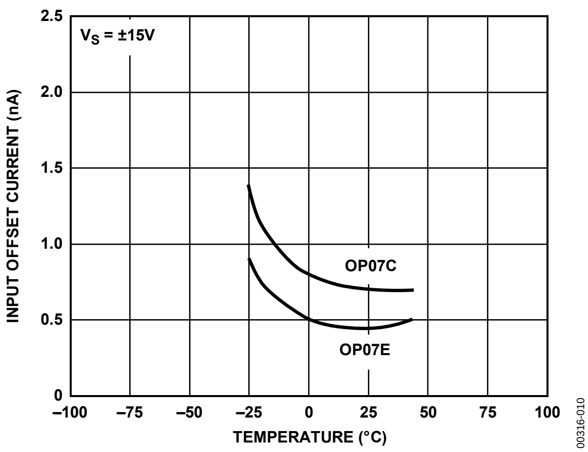


Figure 10. Input Offset Current vs. Temperature

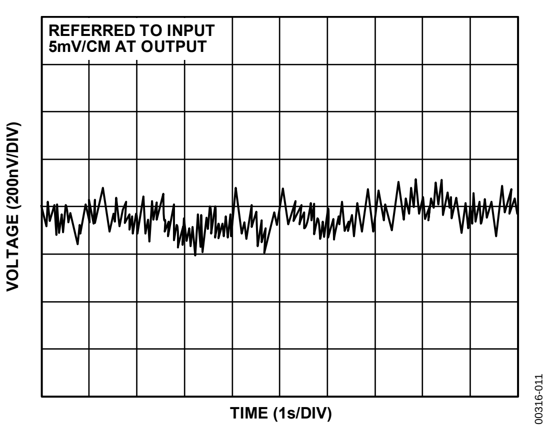


Figure 11. Low Frequency Noise

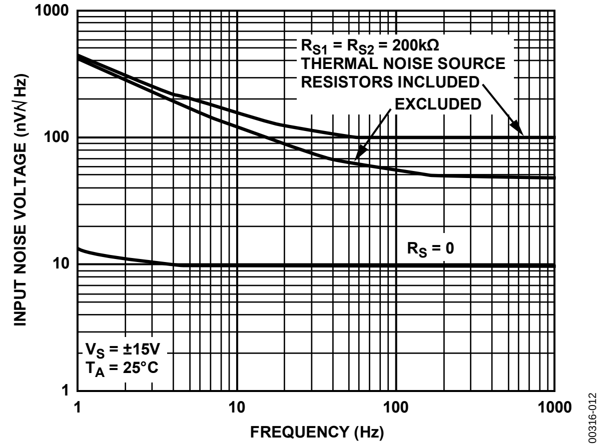


Figure 12. Total Input Noise Voltage vs. Frequency

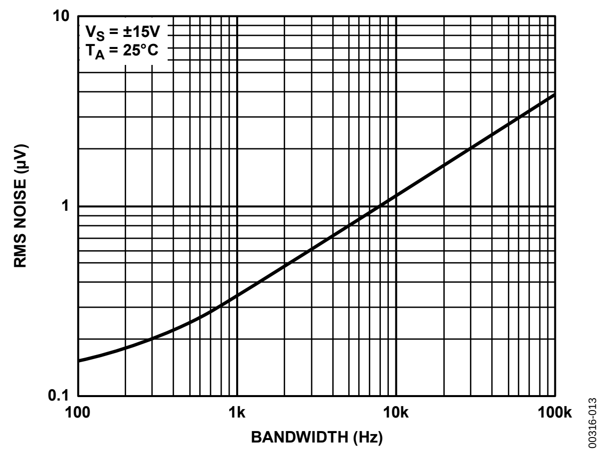


Figure 13. Input Wideband Noise vs. Bandwidth, 0.1 Hz to Frequency Indicated

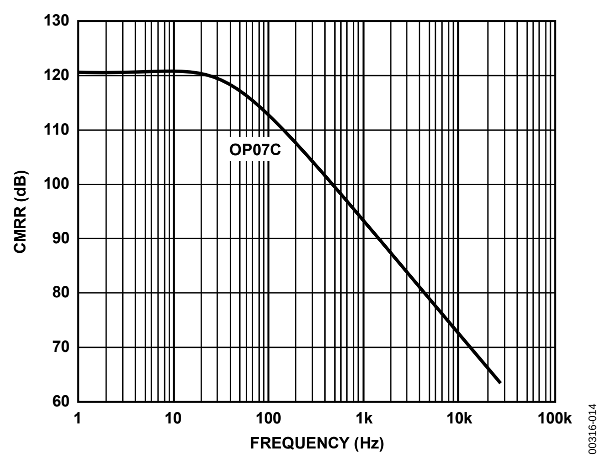


Figure 14. CMRR vs. Frequency

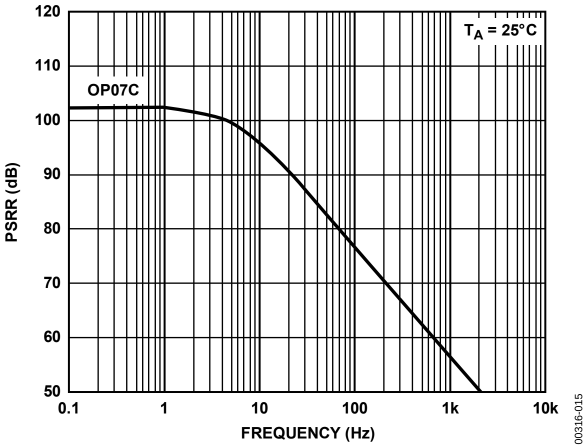


Figure 15. PSRR vs. Frequency

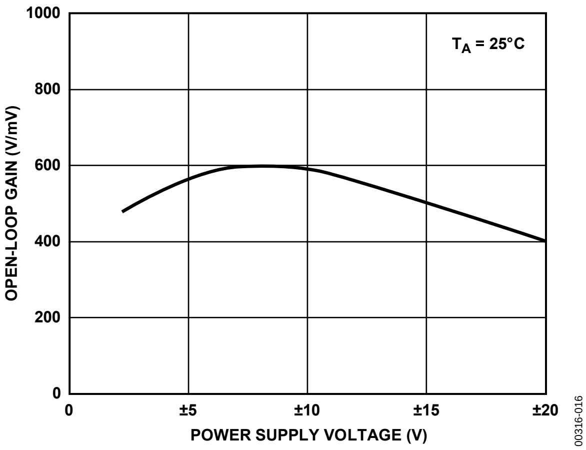


Figure 16. Open-Loop Gain vs. Power Supply Voltage

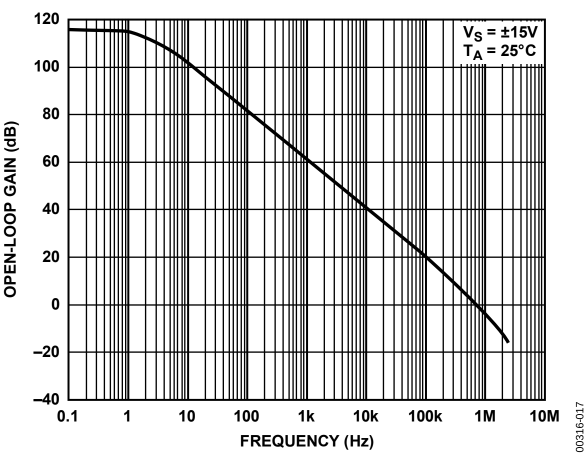


Figure 17. Open-Loop Frequency Response

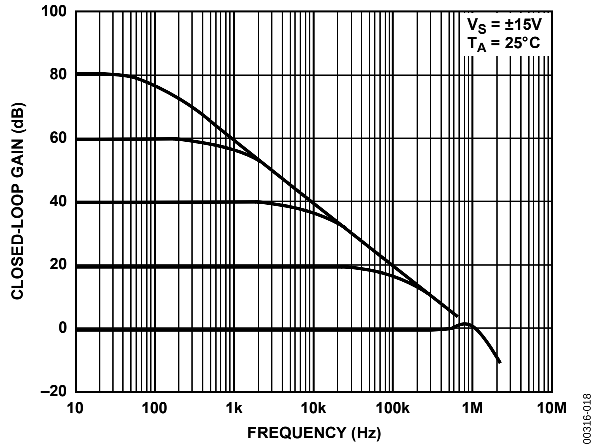


Figure 18. Closed-Loop Frequency Response for Various Gain Configurations

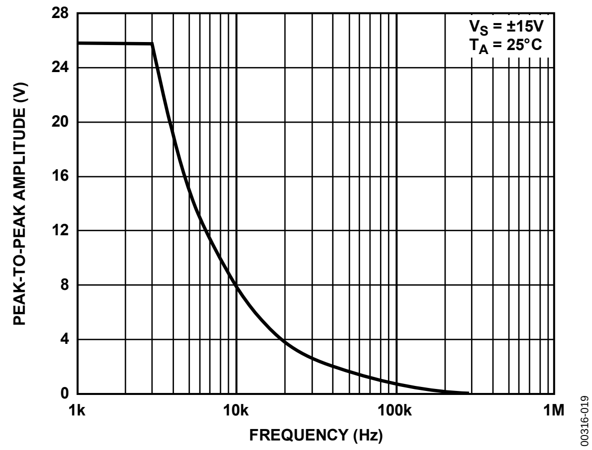


Figure 19. Maximum Output Swing vs. Frequency

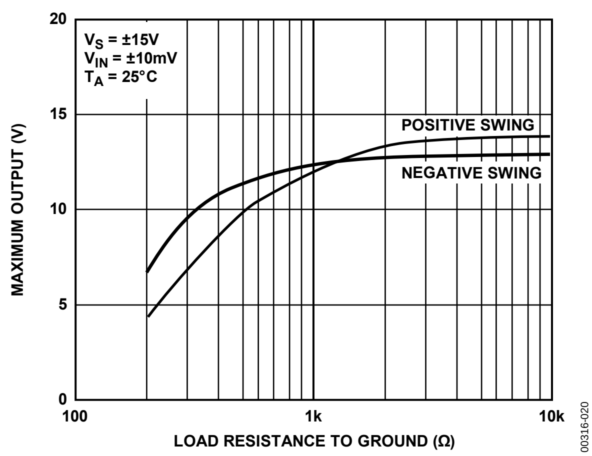


Figure 20. Maximum Output Voltage vs. Load Resistance

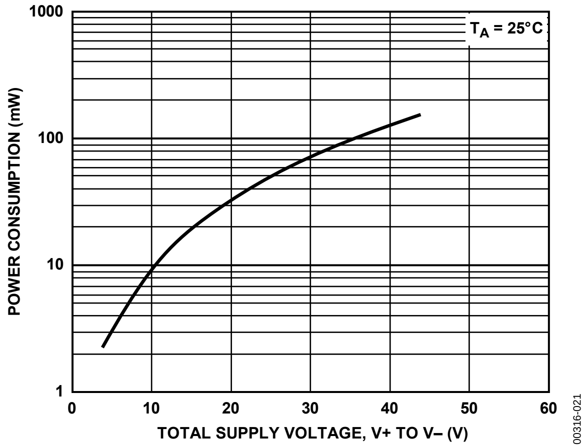


Figure 21. Power Consumption vs. Power Supply

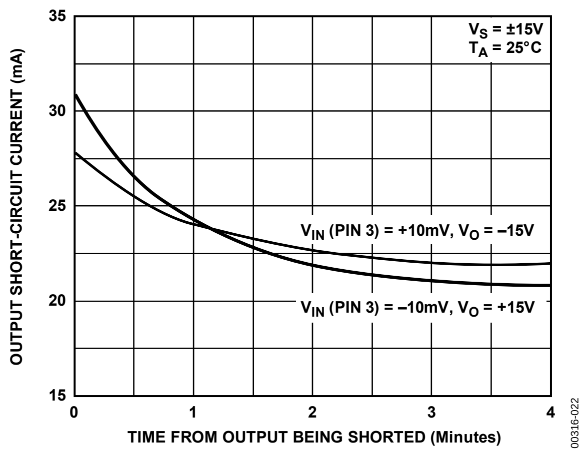


Figure 22. Output Short-Circuit Current vs. Time

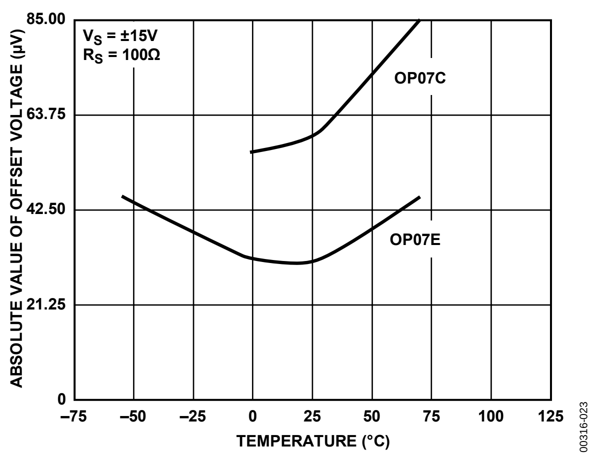


Figure 23. Untrimmed Offset Voltage vs. Temperature

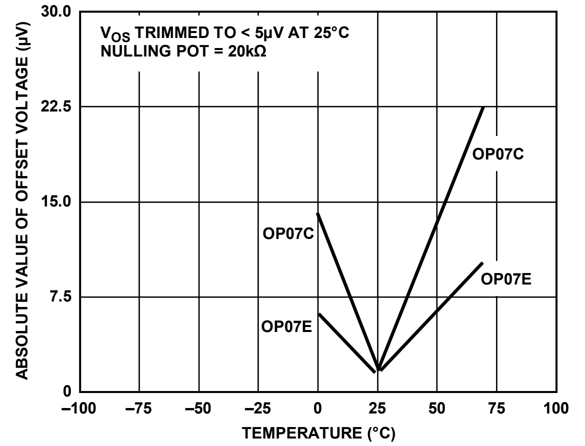


Figure 24. Trimmed Offset Voltage vs. Temperature

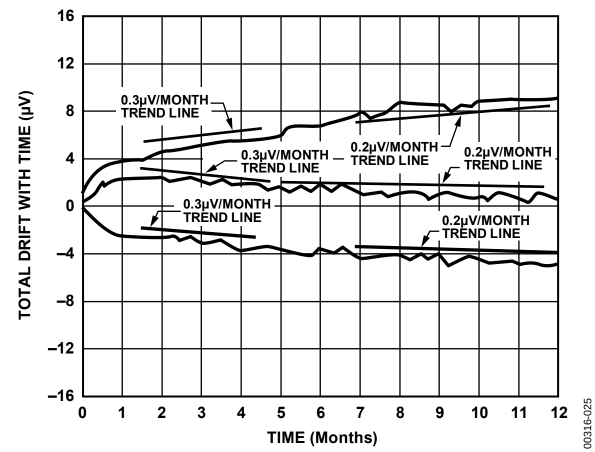


Figure 25. Offset Voltage Drift vs. Time

TYPICAL APPLICATIONS

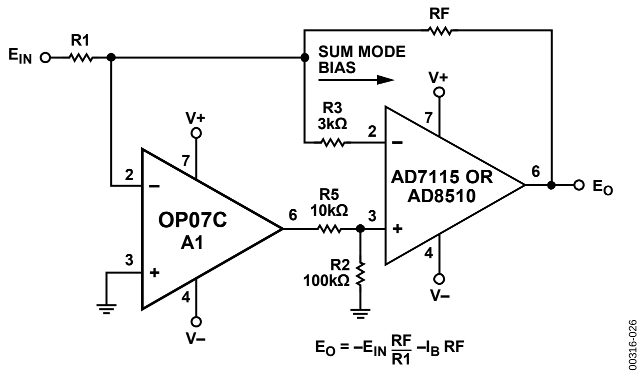


Figure 26. Typical Offset Voltage Test Circuit

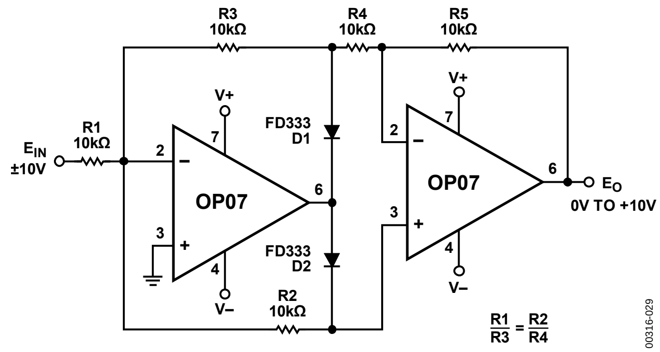


Figure 29. Absolute Value Circuit

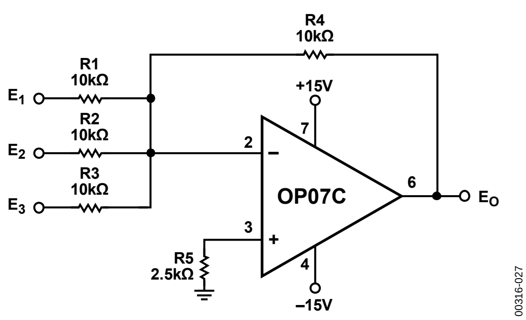


Figure 27. Typical Low Frequency Noise Circuit

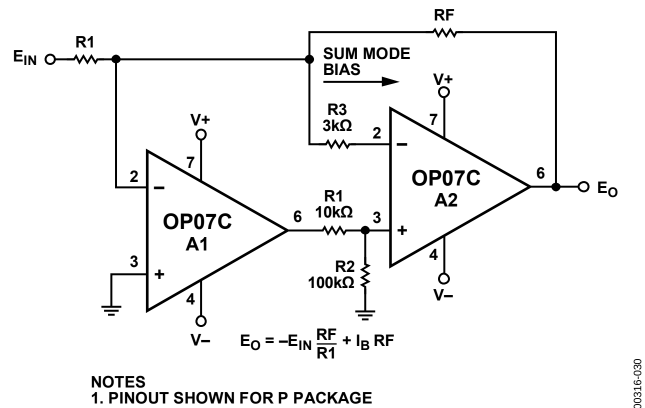


Figure 30. High Speed, Low V_{OS} Composite Amplifier

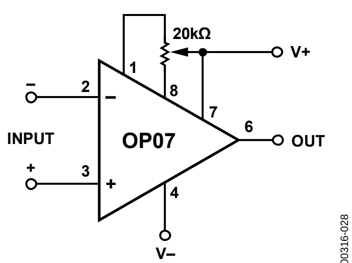


Figure 28. Optional Offset Nulling Circuit

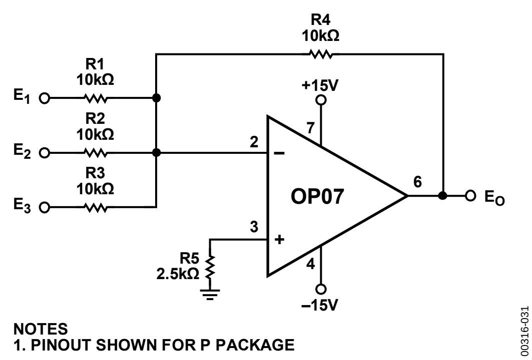


Figure 31. Adjustment-Free Precision Summing Amplifier

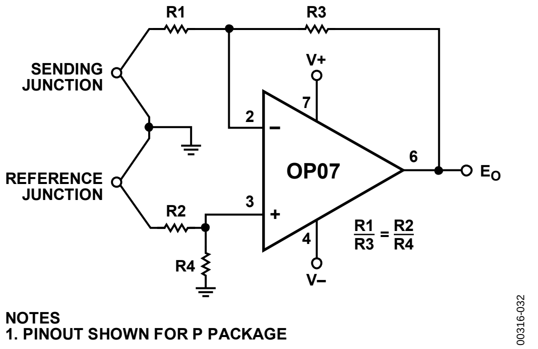


Figure 32. High Stability Thermocouple Amplifier

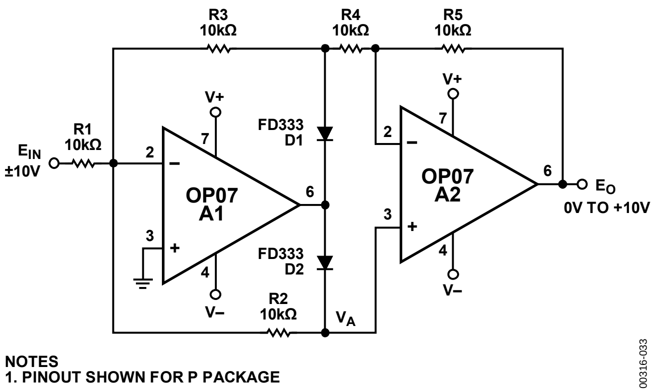


Figure 33. Precision Absolute-Value Circuit

APPLICATIONS INFORMATION

The OP07 provides stable operation with load capacitance of up to 500 pF and ±10 V swings; larger capacitances should be decoupled with a 50 Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation is obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

OUTLINE DIMENSIONS

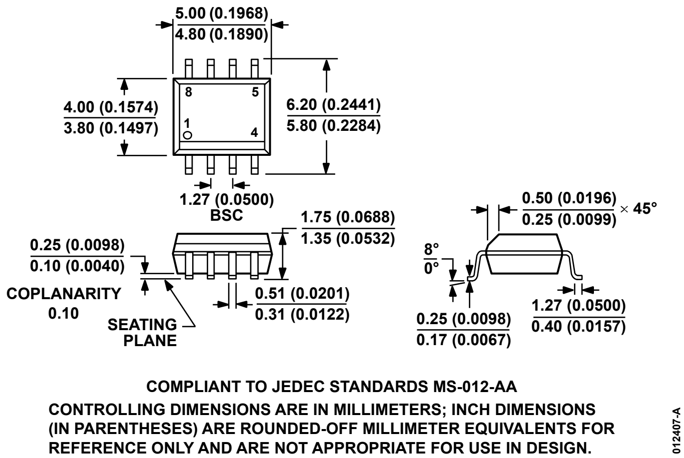


Figure 34. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

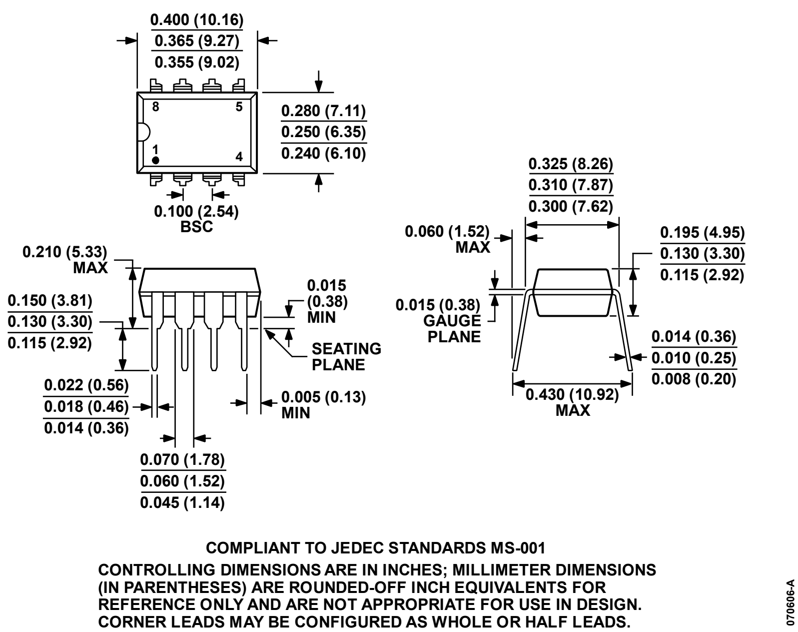


Figure 35. 8-Lead Plastic Dual-in-Line Package [PDIP]
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

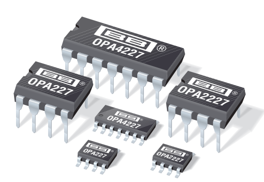
Model[1]	Temperature Range	Package Description	Package Option
OP07EPZ	0°C to 70°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CPZ	−40°C to +85°C	8-Lead PDIP	N-8 (P-Suffix)
OP07CSZ	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)
OP07CSZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8 (S-Suffix)

[1] Z = RoHS Compliant Part.

NOTES

NOTES

Burr-Brown Products
from Texas Instruments



OPA227
OPA2227
OPA4227
OPA228
OPA2228
OPA4228

SBOS110A – MAY 1998 – REVISED JANUARY 2005

High Precision, Low Noise OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 3nV/√Hz
- WIDE BANDWIDTH:
  OPA227: 8MHz, 2.3V/μs
  OPA228: 33MHz, 10V/μs
- SETTLING TIME: 5μs
  (significant improvement over OP-27)
- HIGH CMRR: 138dB
- HIGH OPEN-LOOP GAIN: 160dB
- LOW INPUT BIAS CURRENT: 10nA max
- LOW OFFSET VOLTAGE: 75μV max
- WIDE SUPPLY RANGE: ±2.5V to ±18V
- OPA227 REPLACES OP-27, LT1007, MAX427
- OPA228 REPLACES OP-37, LT1037, MAX437
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

- DATA ACQUISITION
- TELECOM EQUIPMENT
- GEOPHYSICAL ANALYSIS
- VIBRATION ANALYSIS
- SPECTRAL ANALYSIS
- PROFESSIONAL AUDIO EQUIPMENT
- ACTIVE FILTERS
- POWER SUPPLY CONTROL

SPICE model available for OPA227 at www.ti.com

DESCRIPTION

The OPA227 and OPA228 series op amps combine low noise and wide bandwidth with high precision to make them the ideal choice for applications requiring both ac and precision dc performance.

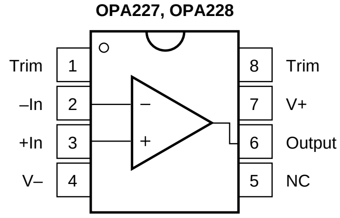
The OPA227 is unity-gain stable and features high slew rate (2.3V/μs) and wide bandwidth (8MHz). The OPA228 is optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10V/μs and a bandwidth of 33MHz.

The OPA227 and OPA228 series op amps are ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPA227 and OPA228 series op amps are pin-for-pin replacements for the industry standard OP-27 and OP-37 with substantial improvements across the board. The dual and quad versions are available for space savings and per-channel cost reduction.

The OPA227, OPA228, OPA2227, and OPA2228 are available in DIP-8 and SO-8 packages. The OPA4227 and OPA4228 are available in DIP-14 and SO-14 packages with standard pin configurations. Operation is specified from –40°C to +85°C.

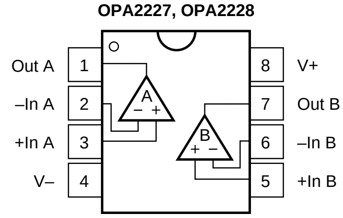
OPA227, OPA228



DIP-8, SO-8

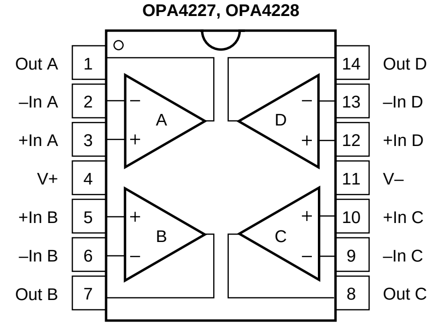
NC = Not Connected

OPA2227, OPA2228



DIP-8, SO-8

OPA4227, OPA4228



DIP-14, SO-14

SPECIFICATIONS: V_S = ±5V to ±15V

OPA227 Series

At T_A = +25°C, and R_L = 10kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA227P, U OPA2227P, U MIN	TYP	MAX	OPA227PA, UA OPA2227PA, UA OPA4227PA, UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±5	±75		±10	±200	μV
T_A = –40°C to +85°C					**±100**			**±200**	μV
vs Temperature	dV_{OS}/dT			**±0.1**	**±0.6**		**±0.3**	**±2**	μV/°C
vs Power Supply	PSRR	V_S = ±2.5V to ±18V		±0.5	±2		*	*	μV/V
T_A = –40°C to +85°C					**±2**			*	μV/V
vs Time				0.2			*		μV/mo
Channel Separation (dual, quad)		dc		0.2			*		μV/V
		f = 1kHz, R_L = 5kΩ		110			*		dB
INPUT BIAS CURRENT									
Input Bias Current	I_B			±2.5	±10		*	*	nA
T_A = –40°C to +85°C					**±10**			*	nA
Input Offset Current	I_{OS}			±2.5	±10		*	*	nA
T_A = –40°C to +85°C					**±10**			*	nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				90			*		nVp-p
				15			*		nVrms
Input Voltage Noise Density, f = 10Hz	e_n			3.5			*		nV/√Hz
f = 100Hz				3			*		nV/√Hz
f = 1kHz				3			*		nV/√Hz
Current Noise Density, f = 1kHz	i_n			0.4			*		pA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}		(V–)+2		(V+)–2	*		*	V
Common-Mode Rejection	CMRR	V_{CM} = (V–)+2V to (V+)–2V	120	138		*	*		dB
T_A = –40°C to +85°C			**120**			*			dB
INPUT IMPEDANCE									
Differential				10^7 || 12			*		Ω || pF
Common-Mode		V_{CM} = (V–)+2V to (V+)–2V		10^9 || 3			*		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	V_O = (V–)+2V to (V+)–2V, R_L = 10kΩ	132	160		*	*		dB
T_A = –40°C to +85°C			**132**			*			dB
		V_O = (V–)+3.5V to (V+)–3.5V, R_L = 600Ω	132	160		*	*		dB
T_A = –40°C to +85°C			**132**			*			dB
FREQUENCY RESPONSE									
Gain Bandwidth Product	GBW			8			*		MHz
Slew Rate	SR			2.3			*		V/μs
Settling Time: 0.1%		G = 1, 10V Step, C_L = 100pF		5			*		μs
0.01%		G = 1, 10V Step, C_L = 100pF		5.6			*		μs
Overload Recovery Time		V_{IN} • G = V_S		1.3			*		μs
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, G = 1, V_O = 3.5Vrms		0.00005			*		%
OUTPUT									
Voltage Output		R_L = 10kΩ	(V–)+2		(V+)–2	*		*	V
T_A = –40°C to +85°C		R_L = 10kΩ	**(V–)+2**		**(V+)–2**	*		*	V
		R_L = 600Ω	(V–)+3.5		(V+)–3.5	*		*	V
T_A = –40°C to +85°C		R_L = 600Ω	**(V–)+3.5**		**(V+)–3.5**	*		*	V
Short-Circuit Current	I_{SC}			±45			*		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve			*		
POWER SUPPLY									
Specified Voltage Range	V_S		±5		±15	*		*	V
Operating Voltage Range			±2.5		±18	*		*	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±3.7	±3.8		*	*	mA
T_A = –40°C to +85°C		I_O = 0			**±4.2**			*	mA
TEMPERATURE RANGE									
Specified Range			–40		+85	*		*	°C
Operating Range			–55		+125	*		*	°C
Storage Range			–65		+150	*		*	°C
Thermal Resistance	θ_{JA}								
SO-8 Surface Mount				150			*		°C/W
DIP-8				100			*		°C/W
DIP-14				80			*		°C/W
SO-14 Surface Mount				100			*		°C/W

* Specifications same as OPA227P, U.

SPECIFICATIONS: V_S = ±5V to ±15V

OPA228 Series

At T_A = +25°C, and R_L = 10kΩ, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

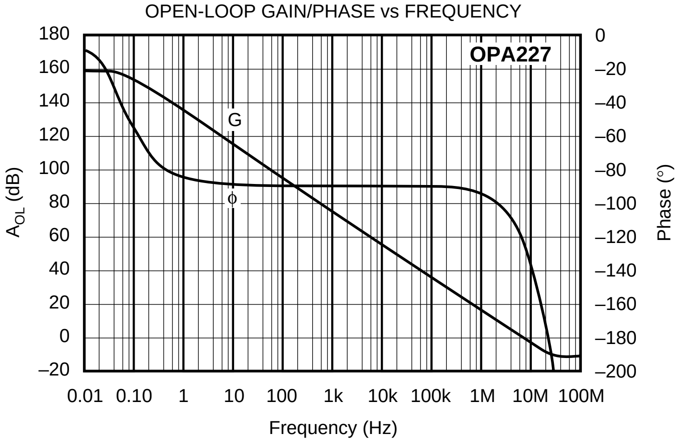
		OPA228P, U OPA2228P, U			OPA228PA, UA OPA2228PA, UA OPA4228PA, UA			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage V_{OS}			±5	±75		±10	±200	μV
T_A = –40°C to +85°C				**±100**			**±200**	μV
vs Temperature dV_{OS}/dT			**±0.1**	**±0.6**		**±0.3**	**±2**	μV/°C
vs Power Supply PSRR	V_S = ±2.5V to ±18V		±0.5	±2		*	*	μV/V
T_A = –40°C to +85°C				**±2**			*	μV/V
vs Time			0.2			*		μV/mo
Channel Separation (dual, quad)	dc		0.2			*		μV/V
	f = 1kHz, R_L = 5kΩ		110			*		dB
INPUT BIAS CURRENT								
Input Bias Current I_B			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
Input Offset Current I_{OS}			±2.5	±10		*	*	nA
T_A = –40°C to +85°C				**±10**			*	nA
NOISE								
Input Voltage Noise, f = 0.1Hz to 10Hz			90			*		nVp-p
			15			*		nVrms
Input Voltage Noise Density, f = 10Hz e_n			3.5			*		nV/√Hz
f = 100Hz			3			*		nV/√Hz
f = 1kHz			3			*		nV/√Hz
Current Noise Density, f = 1kHz i_n			0.4			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range V_{CM}		(V–)+2		(V+)–2	*		*	V
Common-Mode Rejection CMRR	V_{CM} = (V–)+2V to (V+)–2V	120	138		*	*		dB
T_A = –40°C to +85°C		**120**			*			dB
INPUT IMPEDANCE								
Differential			10^7 || 12			*		Ω || pF
Common-Mode	V_{CM} = (V–)+2V to (V+)–2V		10^9 || 3			*		Ω || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain A_{OL}	V_O = (V–)+2V to (V+)–2V, R_L = 10kΩ	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
	V_O = (V–)+3.5V to (V+)–3.5V, R_L = 600Ω	132	160		*	*		dB
T_A = –40°C to +85°C		**132**			*			dB
FREQUENCY RESPONSE								
Minimum Closed-Loop Gain			5			*		V/V
Gain Bandwidth Product GBW			33			*		MHz
Slew Rate SR			11			*		V/μs
Settling Time: 0.1%	G = 5, 10V Step, C_L = 100pF, C_F =12pF		1.5			*		μs
0.01%	G = 5, 10V Step, C_L = 100pF, C_F =12pF		2			*		μs
Overload Recovery Time	V_{IN} • G = V_S		0.6			*		μs
Total Harmonic Distortion + Noise THD+N	f = 1kHz, G = 5, V_O = 3.5Vrms		0.00005			*		%
OUTPUT								
Voltage Output	R_L = 10kΩ	(V–)+2		(V+)–2	*		*	V
T_A = –40°C to +85°C	R_L = 10kΩ	**(V–)+2**		**(V+)–2**	*		*	V
	R_L = 600Ω	(V–)+3.5		(V+)–3.5	*		*	V
T_A = –40°C to +85°C	R_L = 600Ω	**(V–)+3.5**		**(V+)–3.5**	*		*	V
Short-Circuit Current I_{SC}			±45			*		mA
Capacitive Load Drive C_{LOAD}			See Typical Curve			*		
POWER SUPPLY								
Specified Voltage Range V_S		±5		±15	*		*	V
Operating Voltage Range		±2.5		±18	*		*	V
Quiescent Current (per amplifier) I_Q	I_O = 0		±3.7	±3.8		*	*	mA
T_A = –40°C to +85°C	I_O = 0			**±4.2**			*	mA
TEMPERATURE RANGE								
Specified Range		–40		+85	*		*	°C
Operating Range		–55		+125	*		*	°C
Storage Range		–65		+150	*		*	°C
Thermal Resistance θ_{JA}								
SO-8 Surface Mount			150			*		°C/W
DIP-8			100			*		°C/W
DIP-14			80			*		°C/W
SO-14 Surface Mount			100			*		°C/W

* Specifications same as OPA228P, U.

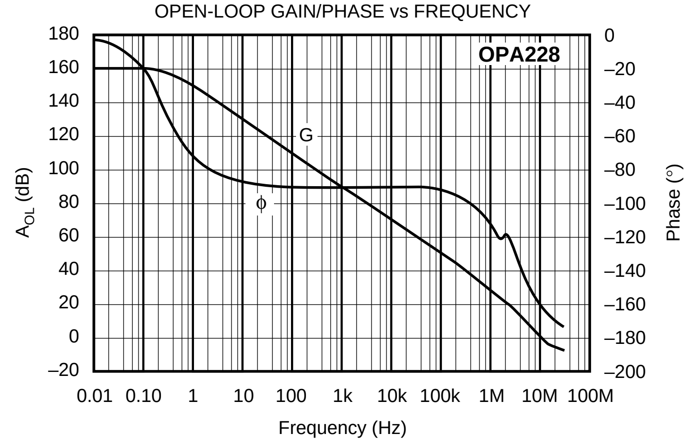
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $R_L = 10kΩ$, and $V_S = ±15V$, unless otherwise noted.

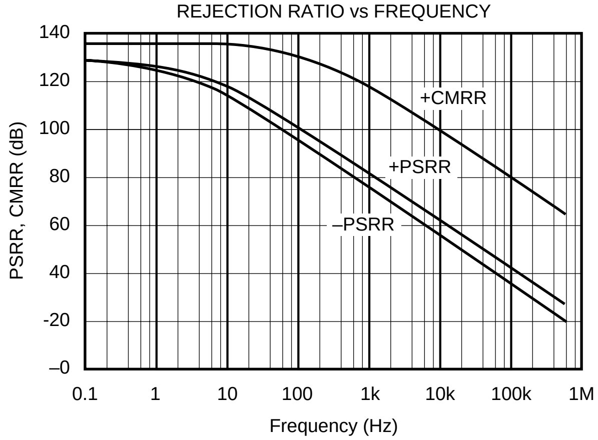
OPEN-LOOP GAIN/PHASE vs FREQUENCY



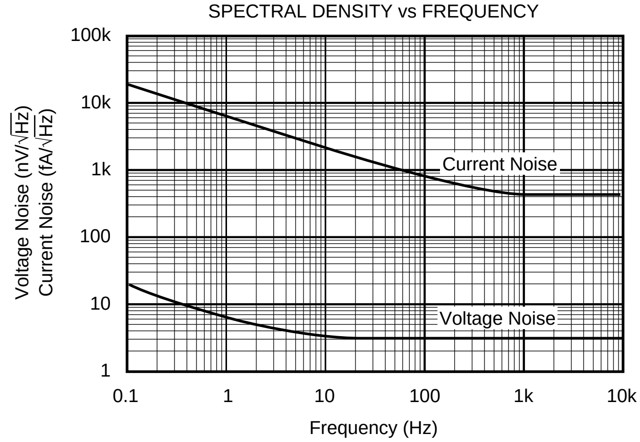
OPEN-LOOP GAIN/PHASE vs FREQUENCY



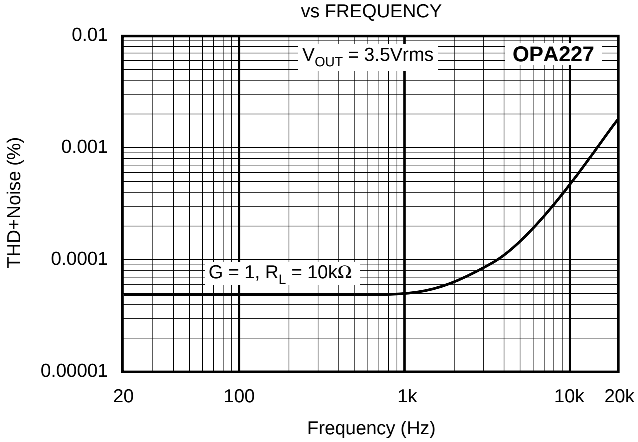
POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



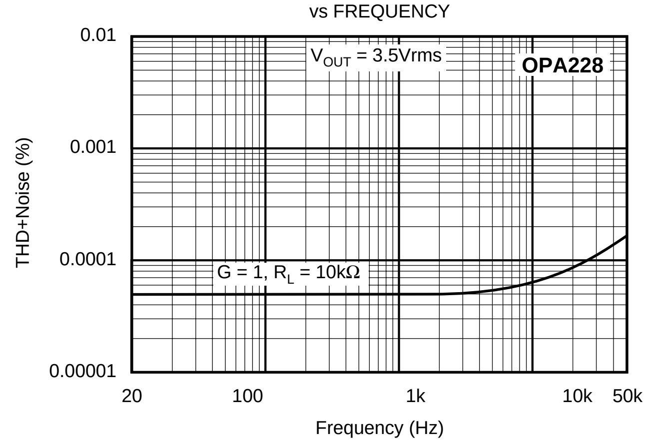
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



APPLICATIONS INFORMATION

The OPA227 and OPA228 series are precision op amps with very low noise. The OPA227 series is unity-gain stable with a slew rate of 2.3V/µs and 8MHz bandwidth. The OPA228 series is optimized for higher-speed applications with gains of 5 or greater, featuring a slew rate of 10V/µs and 33MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

OFFSET VOLTAGE AND DRIFT

The OPA227 and OPA228 series have very low offset voltage and drift. To achieve highest dc precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the op amp inputs which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield op amp and input circuitry from air currents such as those created by cooling fans.

OPERATING VOLTAGE

OPA227 and OPA228 series op amps operate from ±2.5V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA227 series is specified for real-world applications; a single set of specifications applies over the ±5V to ±15V supply range. Specifications are assured for applications between ±5V and ±15V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA227 and OPA228 series can operate with as little as 5V between the supplies and with up to 36V between the supplies. For example, the positive supply could be set to 25V with the negative supply at –5V or vice-versa. In addition, key parameters are assured over the specified temperature range, –40°C to +85°C. Parameters which vary significantly with operating voltage or temperature are shown in the Typical Performance Curves.

OFFSET VOLTAGE ADJUSTMENT

The OPA227 and OPA228 series are laser-trimmed for very low offset and drift so most applications will not require external adjustment. However, the OPA227 and OPA228 (single versions) provide offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp. This adjustment should not be used to compensate for offsets created elsewhere in the system since this can introduce additional temperature drift.

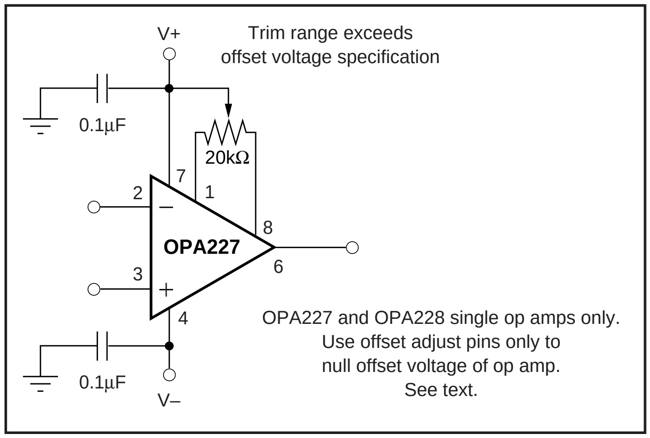


FIGURE 1. OPA227 Offset Voltage Trim Circuit.

INPUT PROTECTION

Back-to-back diodes (see Figure 2) are used for input protection on the OPA227 and OPA228. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier's finite slew rate. Without external current-limiting resistors, the input devices can be destroyed. Sources of high input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

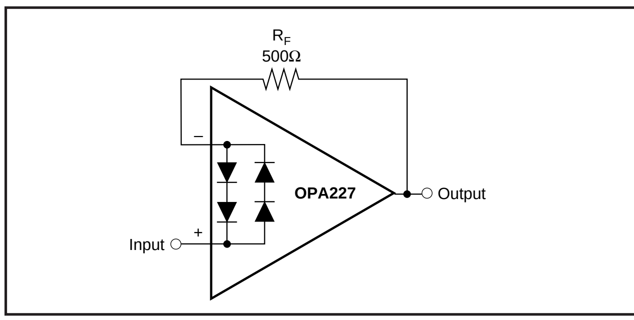


FIGURE 2. Pulsed Operation.

When using the OPA227 as a unity-gain buffer (follower), the input current should be limited to 20mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Sufficient resistor size can be calculated:

$$R_X = V_S/20mA - R_{SOURCE}$$

where R_X is either in series with the source or inserted in the feedback path. For example, for a 10V pulse (V_S = 10V), total loop resistance must be 500Ω. If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen since they will increase noise. See the Noise Performance section of this data sheet for further information on noise calculation. Figure 2 shows an example implementing a current-limiting feedback resistor.

INPUT BIAS CURRENT CANCELLATION

The input bias current of the OPA227 and OPA228 series is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 3) may actually increase offset and noise and is therefore not recommended.

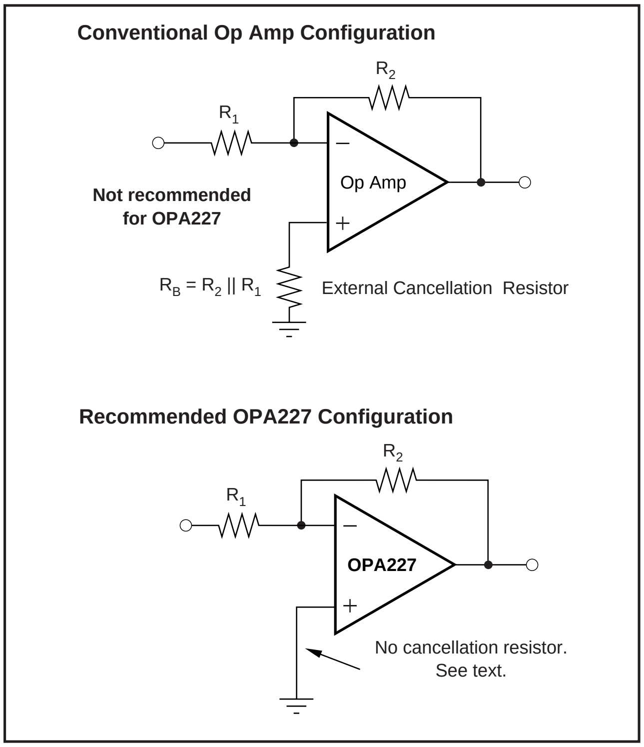


FIGURE 3. Input Bias Current Cancellation.

NOISE PERFORMANCE

Figure 4 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA227 has very low voltage noise, making it ideal for low source impedances (less than 20kΩ). A similar precision op amp, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = $1.38 \cdot 10^{-23}$ J/K and T is temperature in K. For more details on calculating noise, see the insert titled "Basic Noise Calculations."

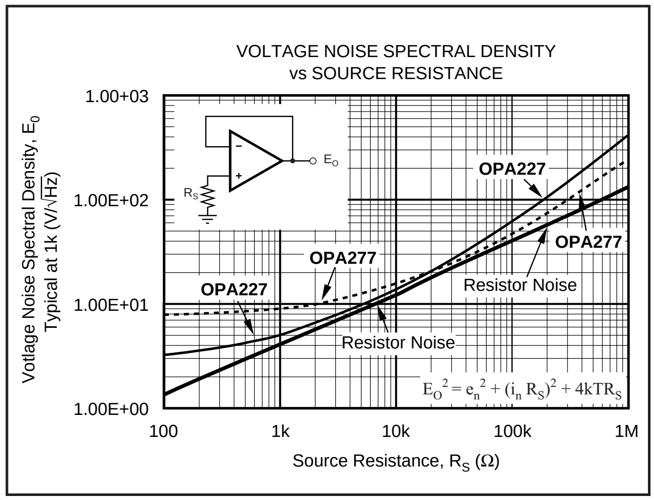


FIGURE 4. Noise Performance of the OPA227 in Unity-Gain Buffer Configuration.

BASIC NOISE CALCULATIONS

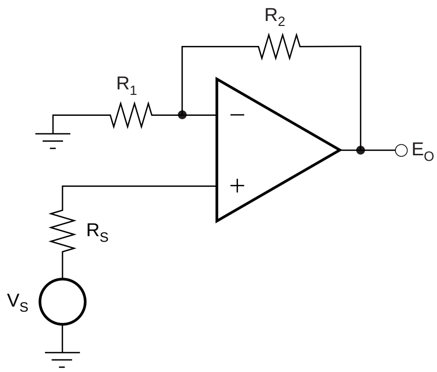
Design of low noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 4. Since the source impedance is usually fixed, select the op amp and the feedback resistors to minimize their contribution to the total noise.

Figure 4 shows total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 5 shows both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Noise in Noninverting Gain Configuration



Noise at the output:

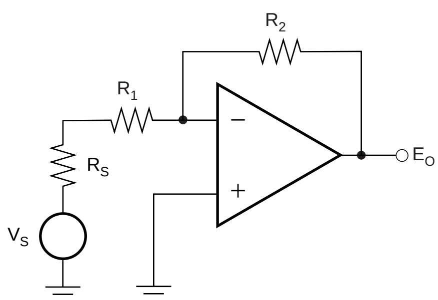
$$E_O^2 = \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + \left(i_n R_2\right)^2 + e_S^2 + \left(i_n R_S\right)^2\left(1+\frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(1+\frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1+\frac{R_2}{R_1+R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + \left(i_n R_2\right)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \bullet \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA227 and OPA228 series op amps at 1kHz, $e_n = 3nV/\sqrt{Hz}$ and $i_n = 0.4pA/\sqrt{Hz}$.

FIGURE 5. Noise Calculation in Gain Configurations.

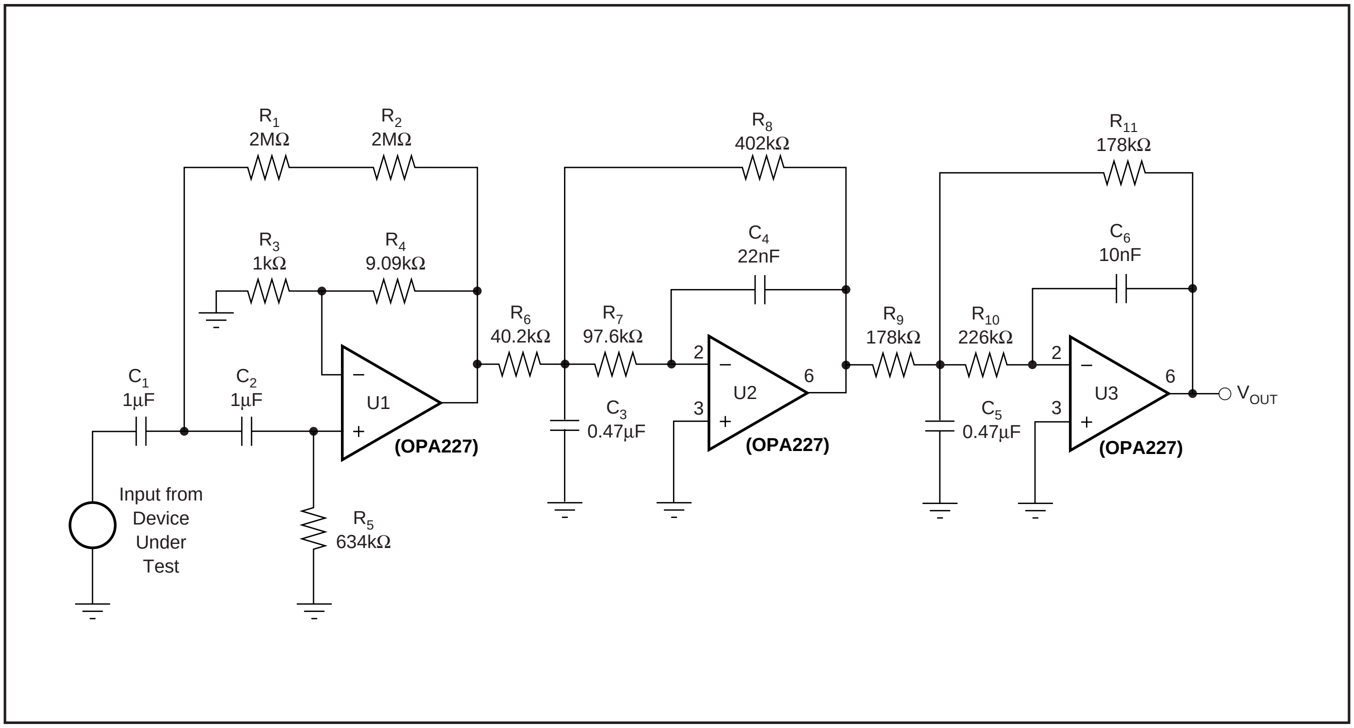


FIGURE 6. 0.1Hz to 10Hz Bandpass Filter Used to Test Wideband Noise of the OPA227 and OPA228 Series.

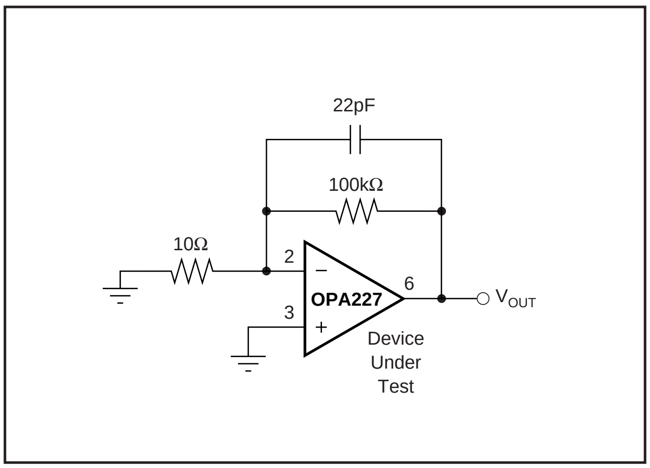


FIGURE 7. Noise Test Circuit.

Figure 6 shows the 0.1Hz 10Hz bandpass filter used to test the noise of the OPA227 and OPA228. The filter circuit was designed using Texas Instruments' FilterPro software (available at www.ti.com). Figure 7 shows the configuration of the OPA227 and OPA228 for noise testing.

USING THE OPA228 IN LOW GAINS

The OPA228 family is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of their high speed in lower gains. Without external compensation, the OPA228 has sufficient phase margin to maintain stability in unity gain with purely resistive loads. However, the addition of load capacitance can reduce the phase margin and destabilize the op amp.

A variety of compensation techniques have been evaluated specifically for use with the OPA228. The recommended configuration consists of an additional capacitor (C_F) in parallel with the feedback resistance, as shown in Figures 8 and 11. This feedback capacitor serves two purposes in compensating the circuit. The op amp's input capacitance and the feedback resistors interact to cause phase shift that can result in instability. C_F compensates the input capacitance, minimizing peaking. Additionally, at high frequencies, the closed-loop gain of the amplifier is strongly influenced by the ratio of the input capacitance and the feedback capacitor. Thus, C_F can be selected to yield good stability while maintaining high speed.

Without external compensation, the noise specification of the OPA228 is the same as that for the OPA227 in gains of 5 or greater. With the additional external compensation, the output noise of the of the OPA228 will be higher. The amount of noise increase is directly related to the increase in high frequency closed-loop gain established by the C_{IN}/C_F ratio.

Figures 8 and 11 show the recommended circuit for gains of +2 and –2, respectively. The figures suggest approximate values for C_F. Because compensation is highly dependent on circuit design, board layout, and load conditions, C_F should be optimized experimentally for best results. Figures 9 and 10 show the large- and small-signal step responses for the G = +2 configuration with 100pF load capacitance. Figures 12 and 13 show the large- and small-signal step responses for the G = –2 configuration with 100pF load capacitance.

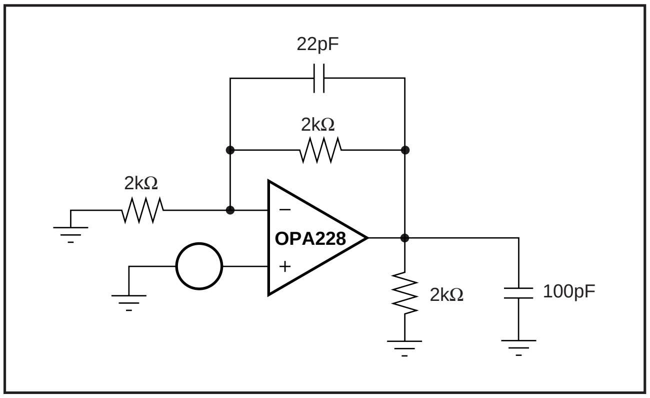


FIGURE 8. Compensation of the OPA228 for G =+2.

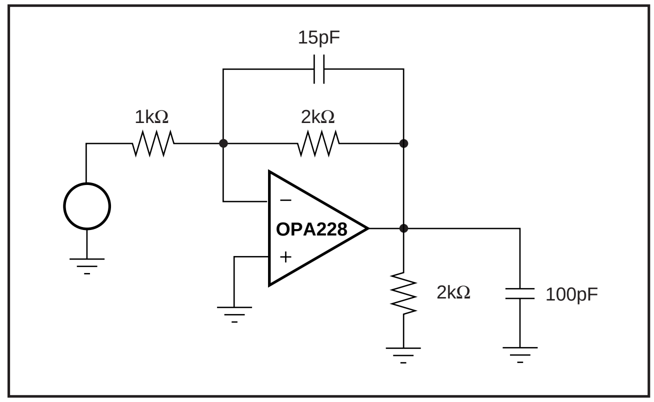


FIGURE 11. Compensation for OPA228 for G = –2.

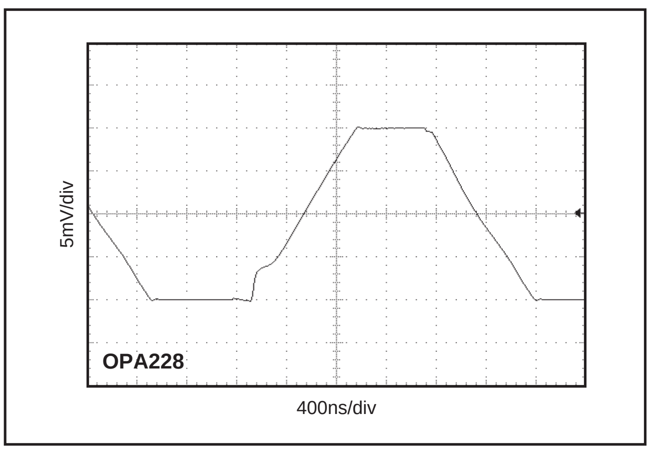


FIGURE 9. Large-Signal Step Response, G = +2, C_{LOAD} = 100pF, Input Signal = 5Vp-p.

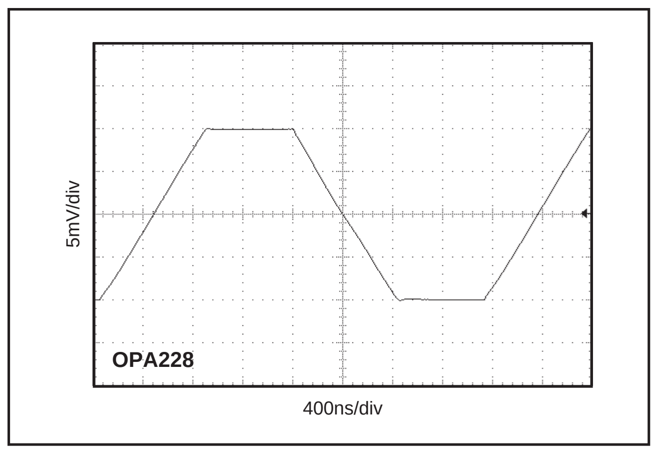


FIGURE 12. Large-Signal Step Response, G = –2, C_{LOAD} = 100pF, Input Signal = 5Vp-p.

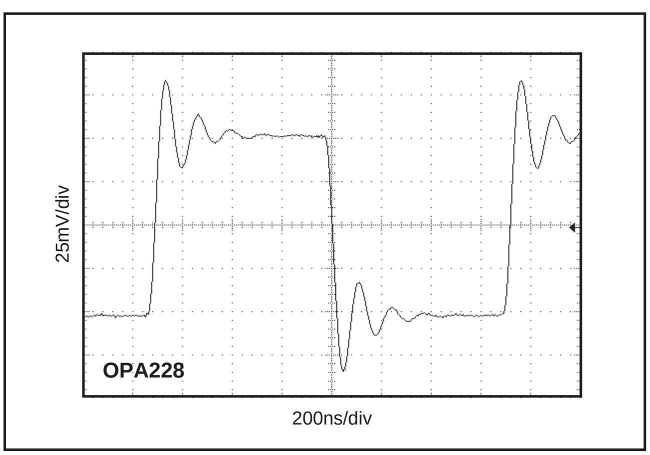


FIGURE 10. Small-Signal Step Response, G = +2, C_{LOAD} = 100pF, Input Signal = 50mVp-p.

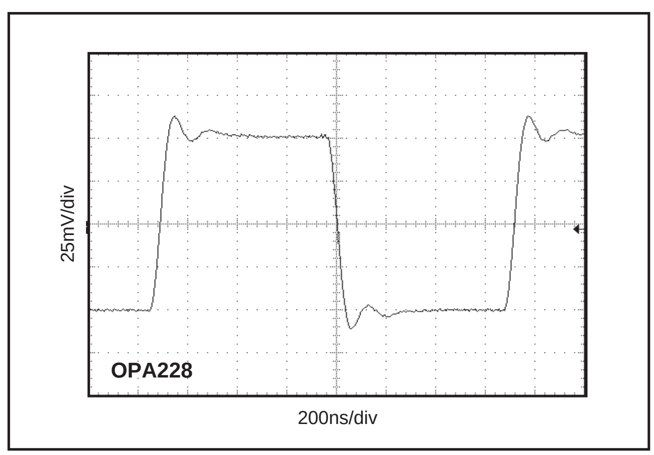


FIGURE 13. Small-Signal Step Response, G = –2, C_{LOAD} = 100pF, Input Signal = 50mVp-p.

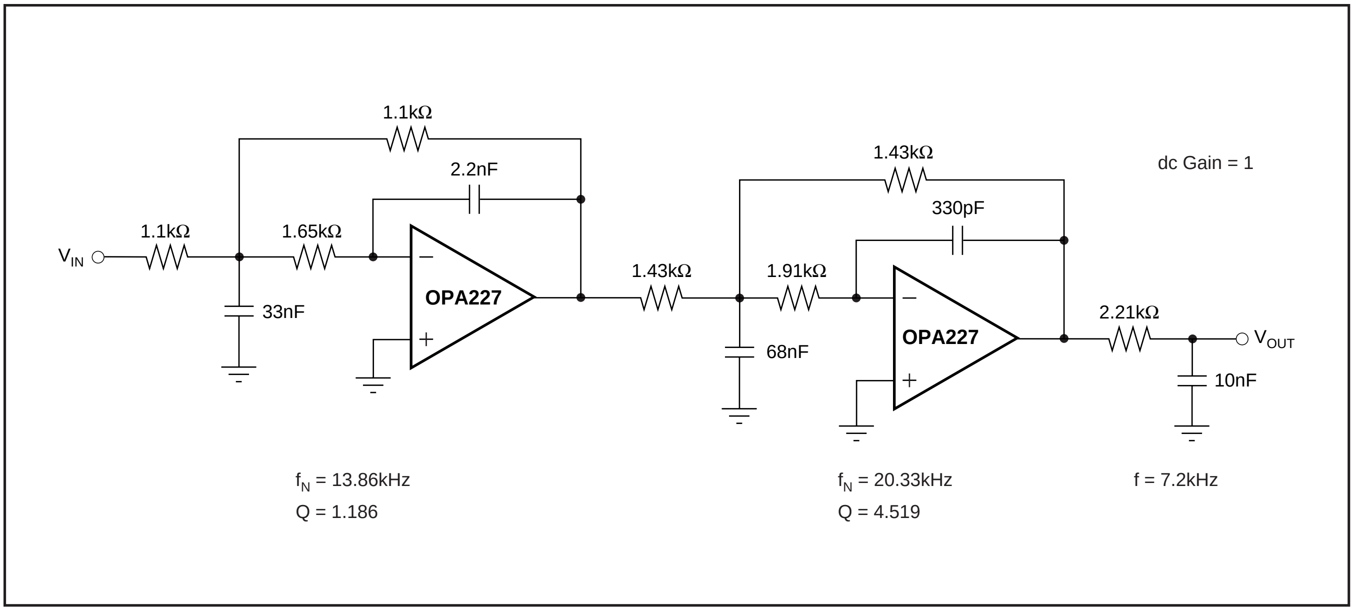


FIGURE 14. Three-Pole, 20kHz Low Pass, 0.5dB Chebyshev Filter.

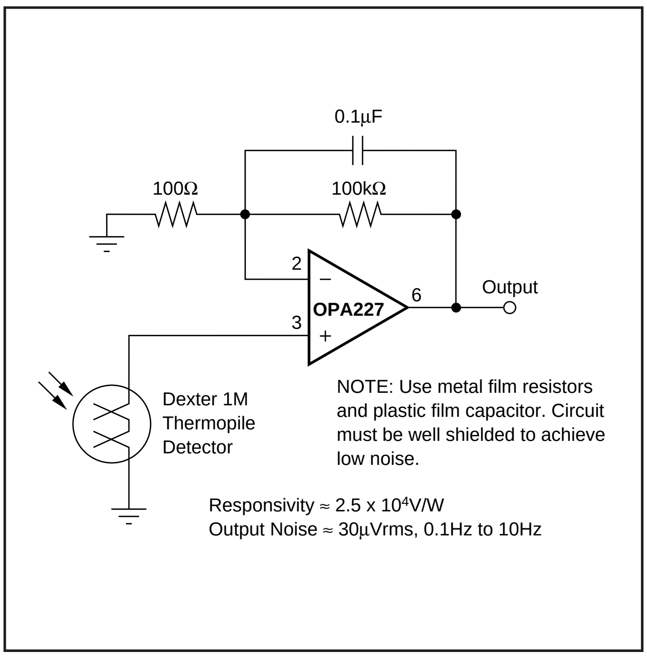


FIGURE 15. Long-Wavelength Infrared Detector Amplifier.

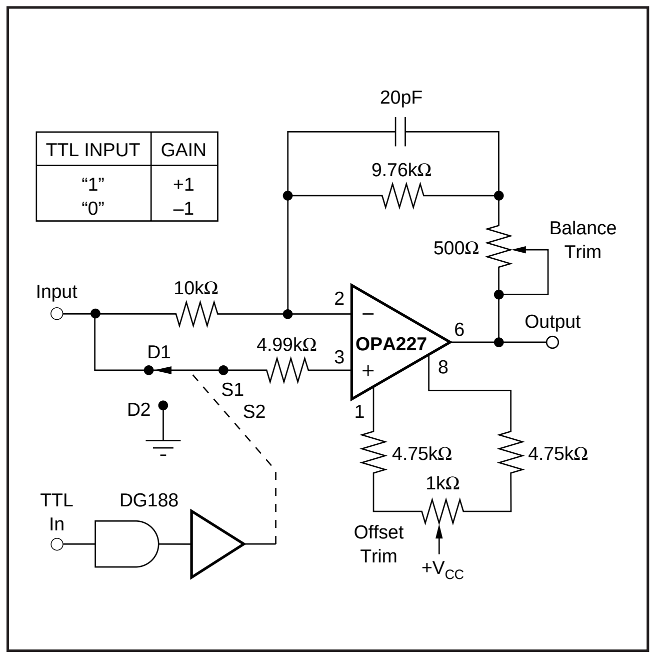


FIGURE 16. High Performance Synchronous Demodulator.

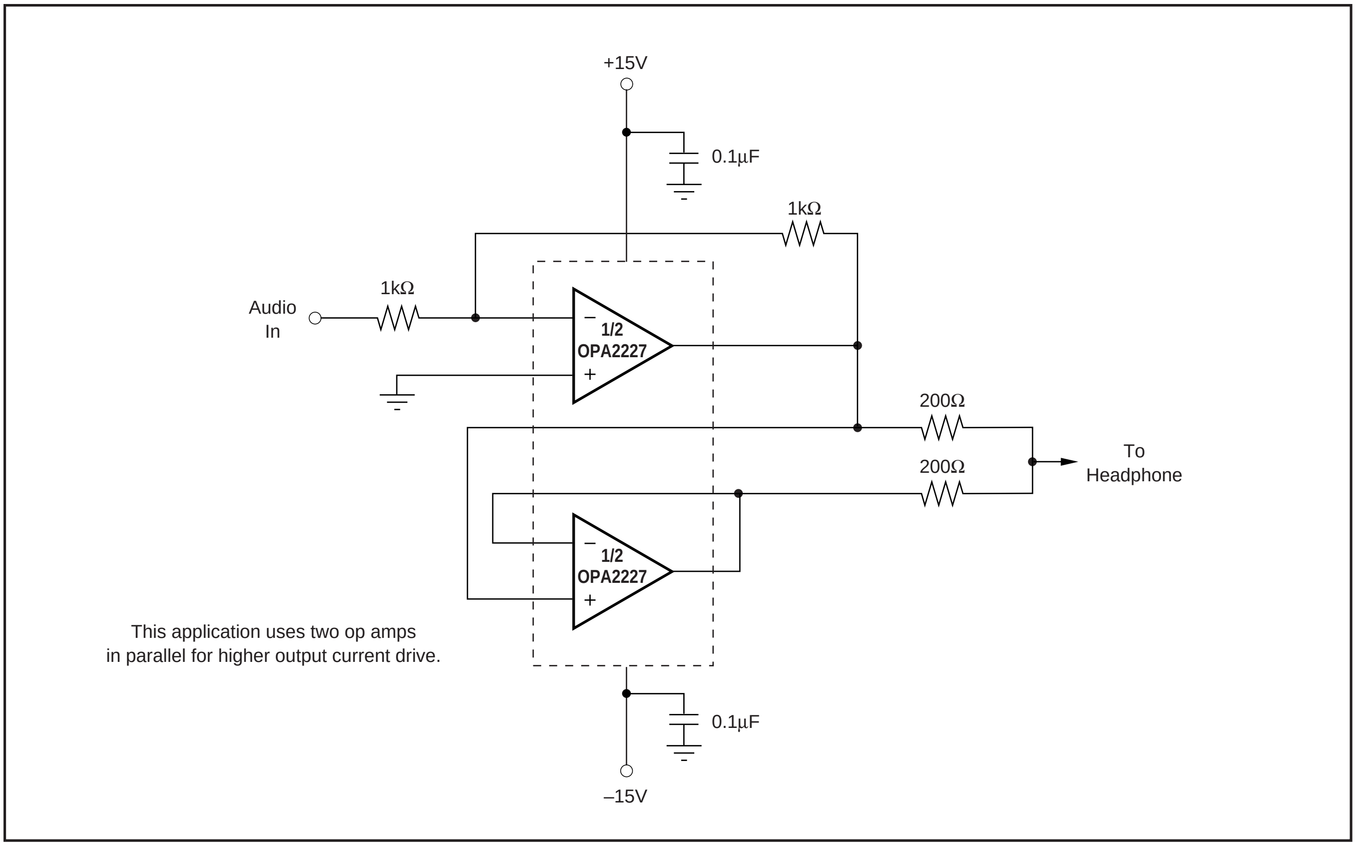


FIGURE 17. Headphone Amplifier.

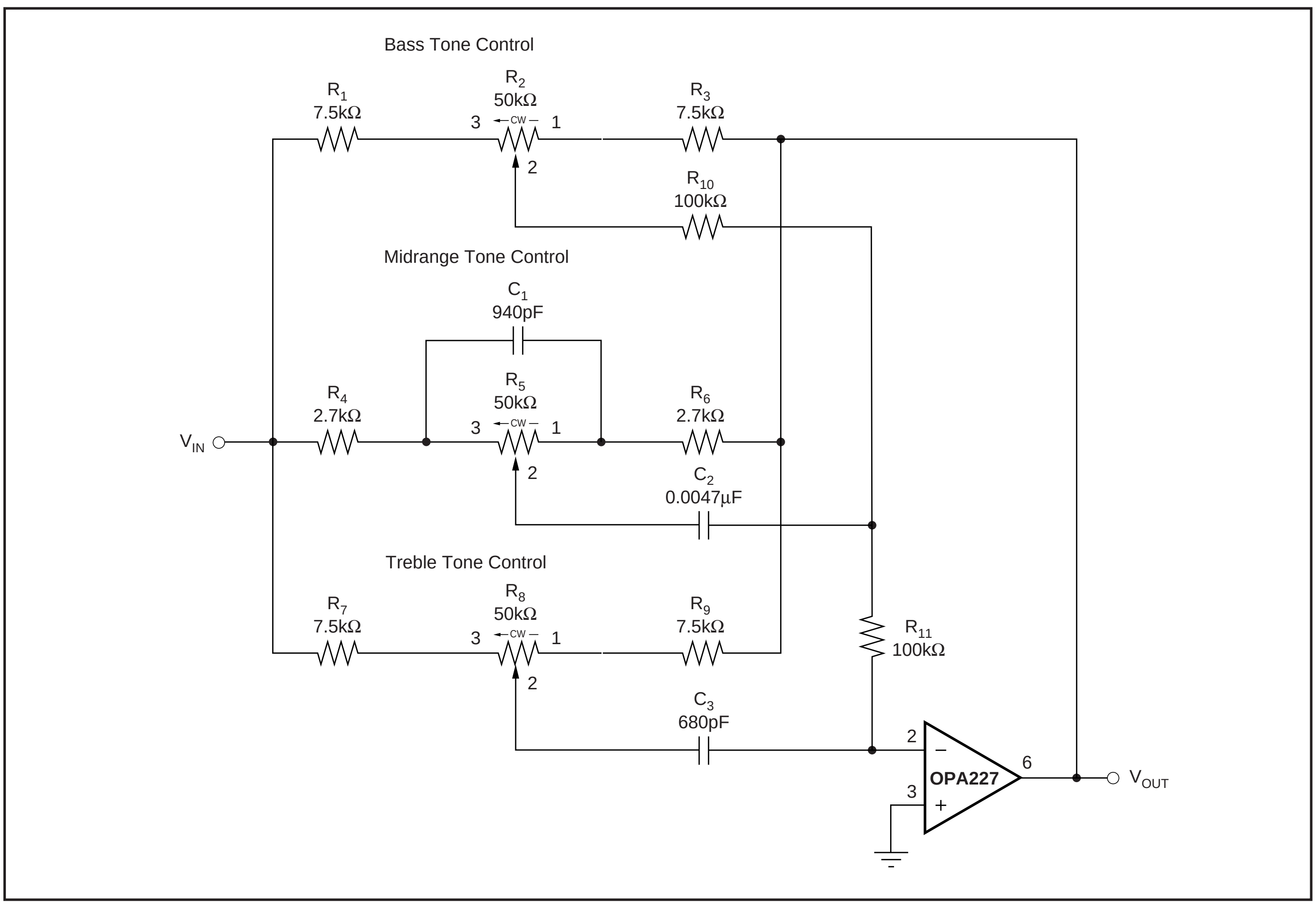


FIGURE 18. Three-Band ActiveTone Control (bass, midrange and treble).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2227U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2227UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
OPA2228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA2228U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA2228UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA227U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA227UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA227UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA228U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA228UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4227PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA4227PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA4227UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4227UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4227UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
OPA4227UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4228PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA4228PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	Add to cart
OPA4228UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4228UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4228UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart
OPA4228UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Add to cart

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

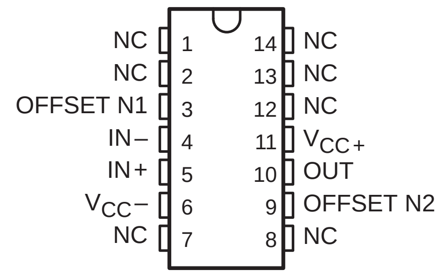
[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

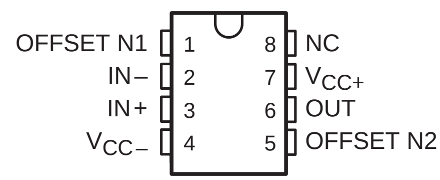
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild µA741**

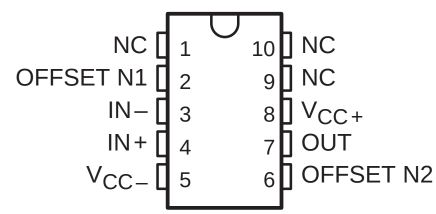
µA741M . . . J PACKAGE
(TOP VIEW)



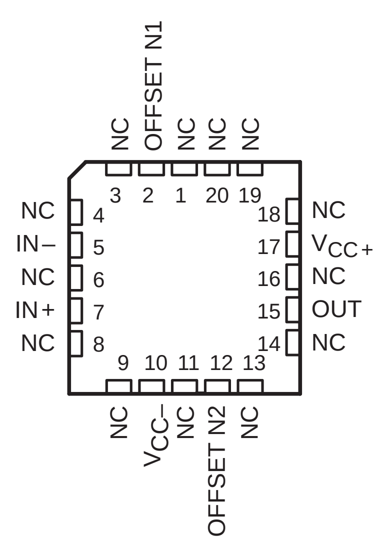
µA741M . . . JG PACKAGE
µA741C, µA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



µA741M . . . U PACKAGE
(TOP VIEW)



µA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

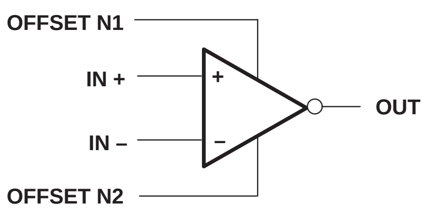
description

The µA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The µA741C is characterized for operation from 0°C to 70°C. The µA741I is characterized for operation from –40°C to 85°C.The µA741M is characterized for operation over the full military temperature range of –55°C to 125°C.

symbol

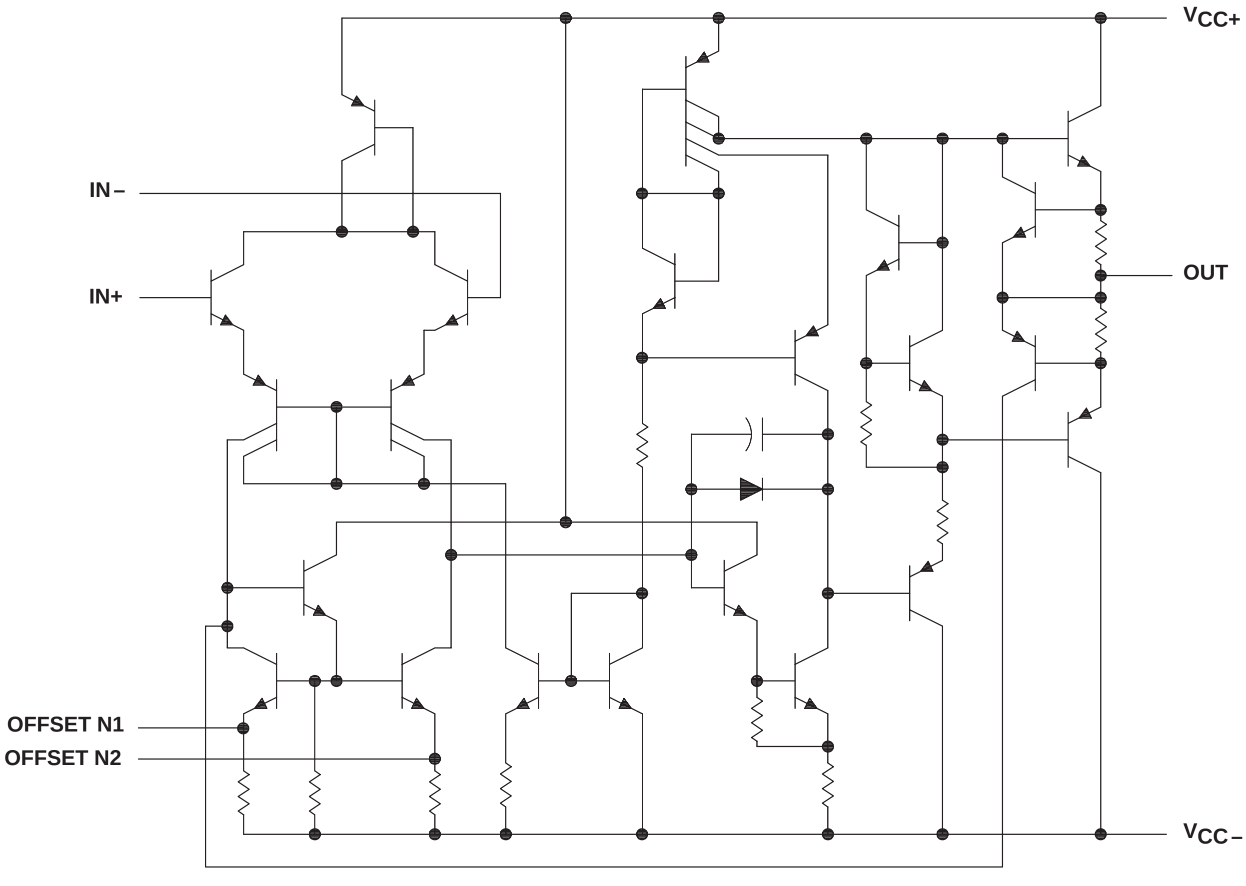


AVAILABLE OPTIONS

T_A	PACKAGED DEVICES							CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	
0°C to 70°C	μA741CD				μA741CP	μA741CPW		μA741Y
–40°C to 85°C	μA741ID				μA741IP			
–55°C to 125°C		μA741MFK	μA741MJ	μA741MJG			μA741MU	

The D package is available taped and reeled. Add the suffix R (e.g., μA741CDR).

schematic



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		μA741C	μA741I	μA741M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	22	V
Supply voltage, V_{CC-} (see Note 1)		–18	–22	–22	V
Differential input voltage, V_{ID} (see Note 2)		±15	±30	±30	V
Input voltage, V_I any input (see Notes 1 and 3)		±15	±15	±15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-}		±15	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		0 to 70	–40 to 85	–55 to 125	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, P, or PW package	260	260		°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	μA741C			μA741I, μA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		±15			±15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L = 2$ kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq 2$ kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ	25°C	20	200		50	200		V/mV
		$V_O = \pm10$ V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm9$ V to ±15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	$V_O = 0$, No load	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the μA741C is 0°C to 70°C, the μA741I is –40°C to 85°C, and the μA741M is –55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	μA741C			μA741I, μA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$		1	6	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$		±15		mV
I_{IO}	Input offset current	$V_O = 0$		20	200	nA
I_{IB}	Input bias current	$V_O = 0$		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	±12	±14		V
		$R_L = 2$ kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm9$ V to ±15 V		30	150	μV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	$V_O = 0$, No load		1.7	2.8	mA
P_D	Total power dissipation	$V_O = 0$, No load		50	85	mW

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

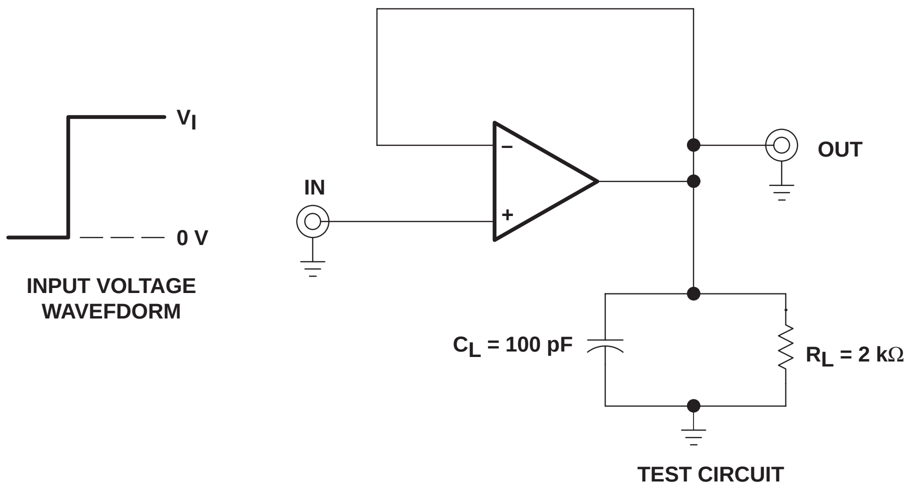


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

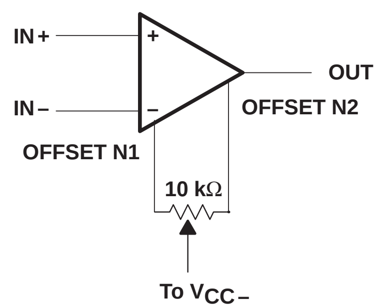


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

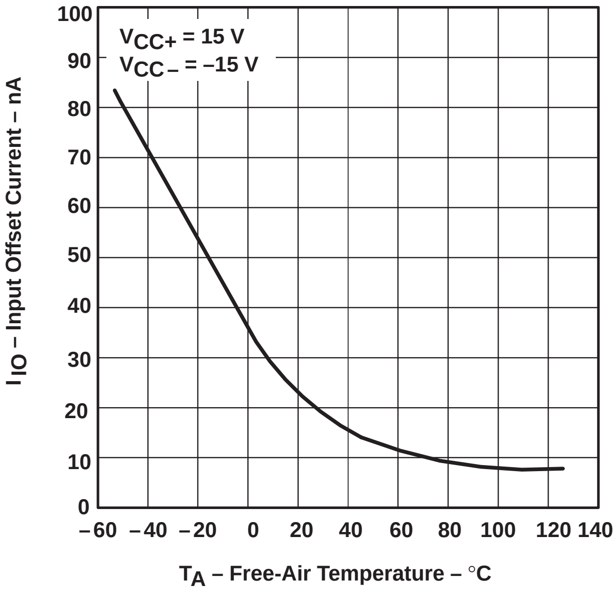


Figure 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

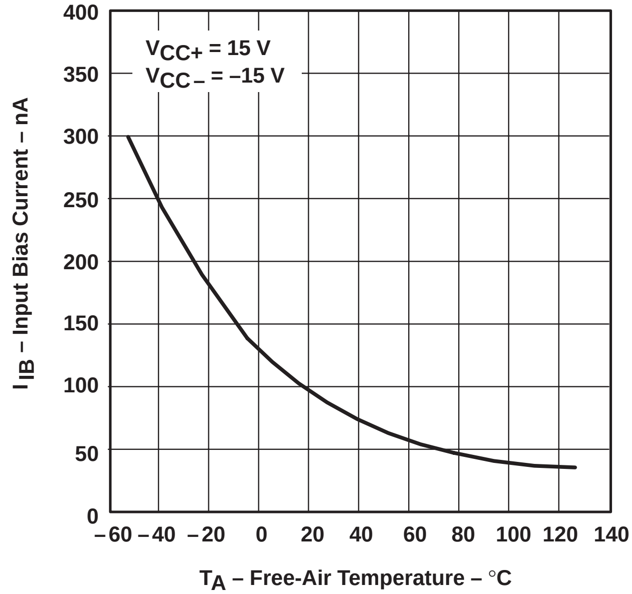


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

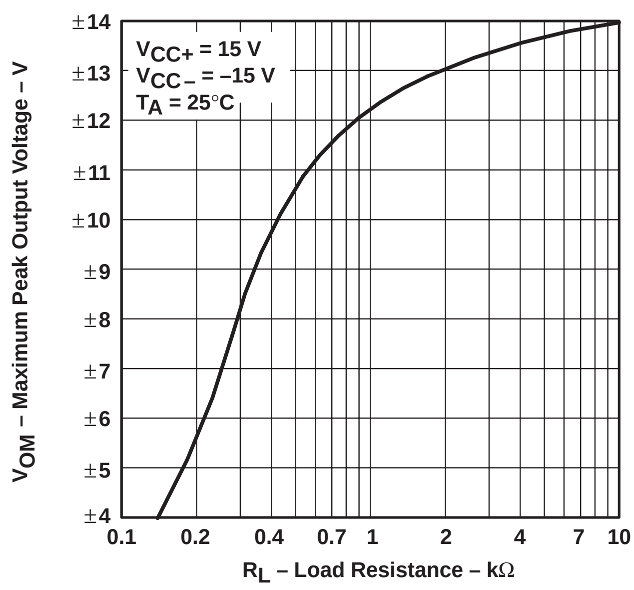


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

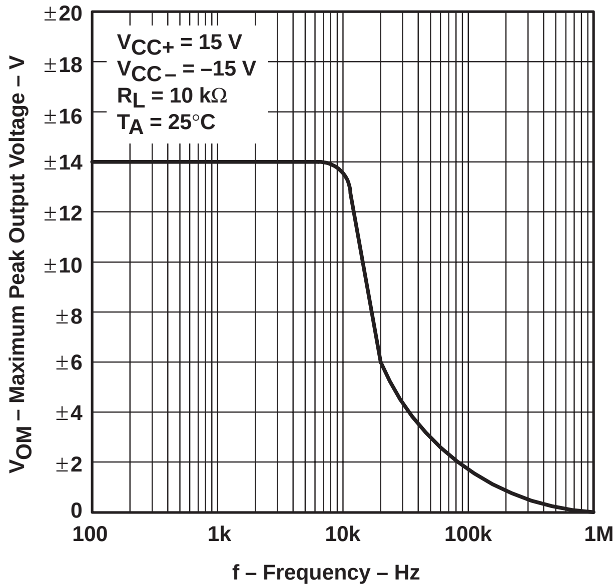


Figure 6

OPEN-LOOP SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

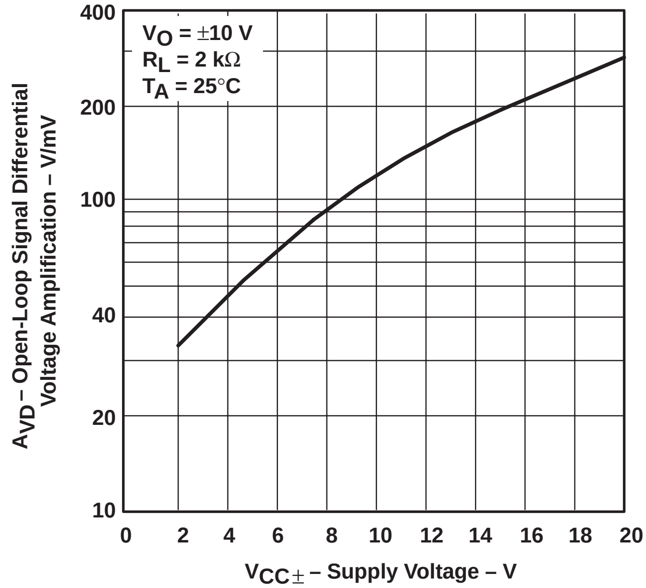
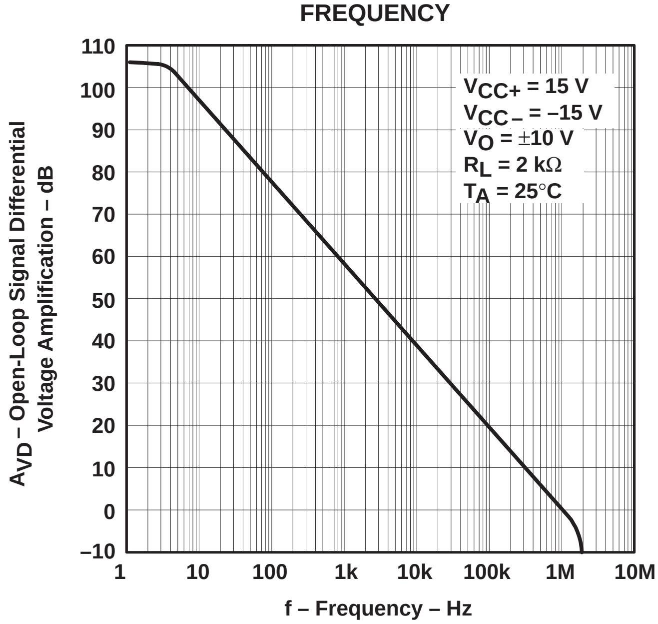


Figure 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

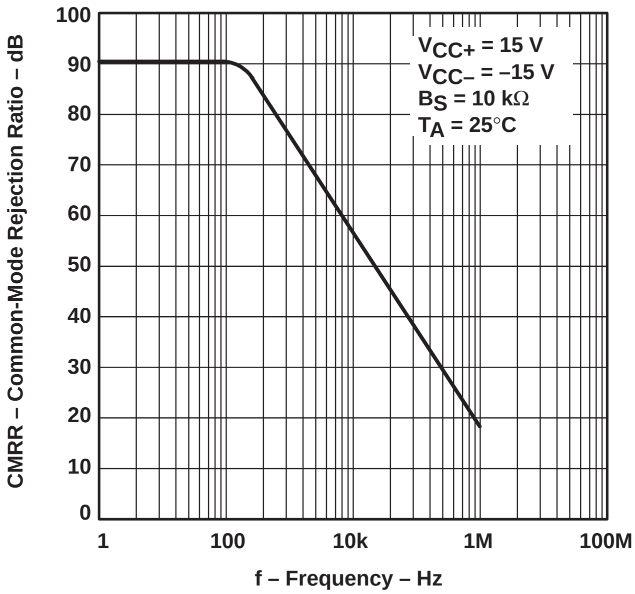


Figure 8

OUTPUT VOLTAGE vs ELAPSED TIME

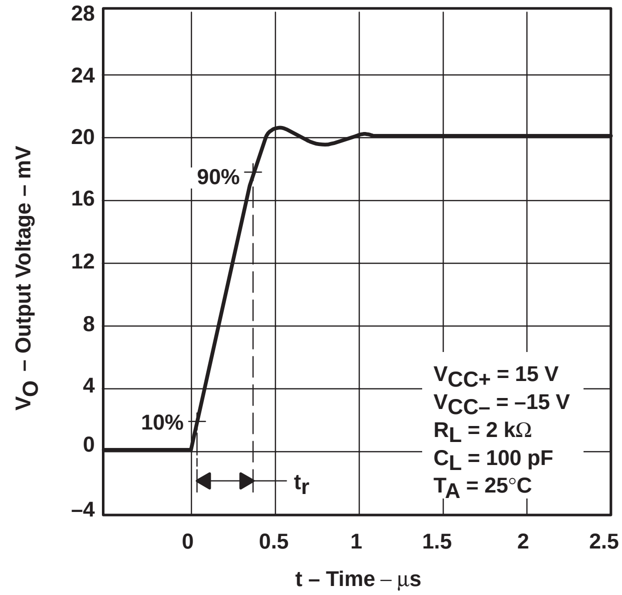


Figure 9

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

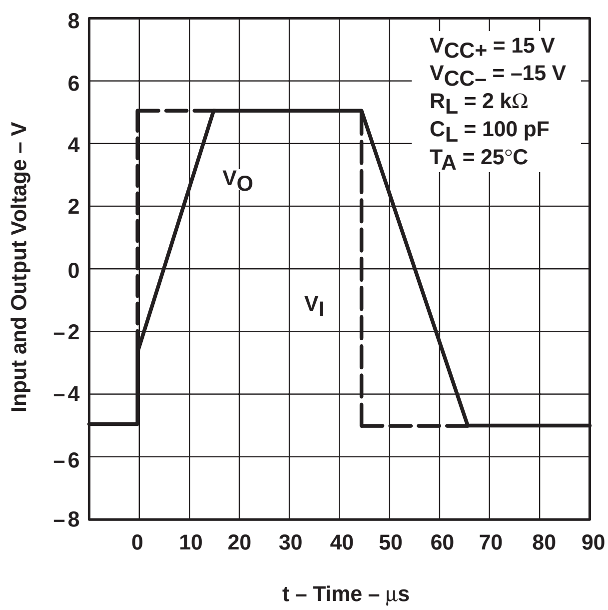
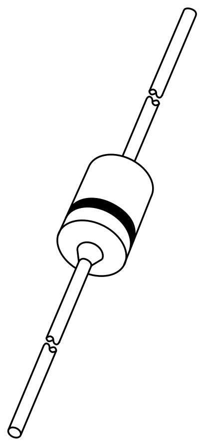


Figure 10

DATA SHEET



1N4148; 1N4446; 1N4448
High-speed diodes

Product specification
Supersedes data of April 1996
File under Discrete Semiconductors, SC01

1996 Sep 03

Philips
Semiconductors

PHILIPS

High-speed diodes 1N4148; 1N4446; 1N4448

FEATURES

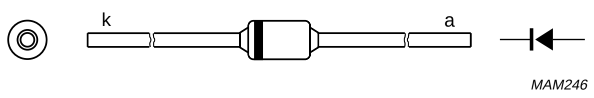
- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 75 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

- High-speed switching.

DESCRIPTION

The 1N4148, 1N4446, 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.



The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	75	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	non-repetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 µs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

ELECTRICAL CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	see Fig.3			
	1N4148	I_F = 10 mA	–	1.0	V
	1N4446	I_F = 20 mA	–	1.0	V
	1N4448	I_F = 5 mA	0.62	0.72	V
		I_F = 100 mA	–	1.0	V
I_R	reverse current	V_R = 20 V; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	–	50	µA
I_R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	–	3	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0; see Fig.6		4	pF
t_{rr}	reverse recovery time	when switched from I_F = 10 mA to I_R = 60 mA; R_L = 100 Ω; measured at I_R = 1 mA; see Fig.7		4	ns
V_{fr}	forward recovery voltage	when switched from I_F = 50 mA; t_r = 20 ns; see Fig.8	–	2.5	V

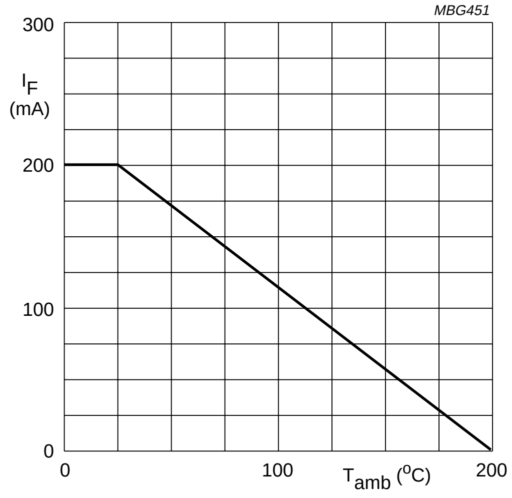
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

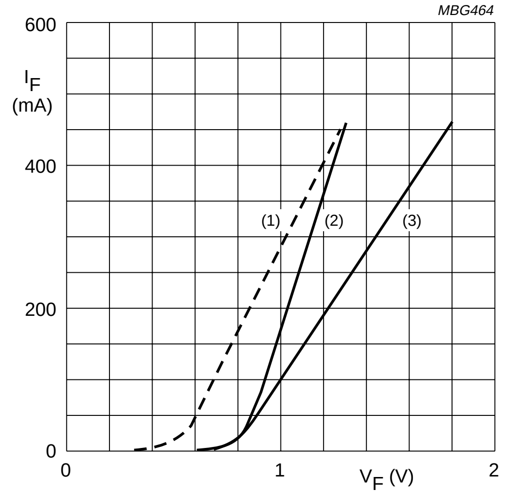
1. Device mounted on a printed circuit-board without metallization pad.

GRAPHICAL DATA



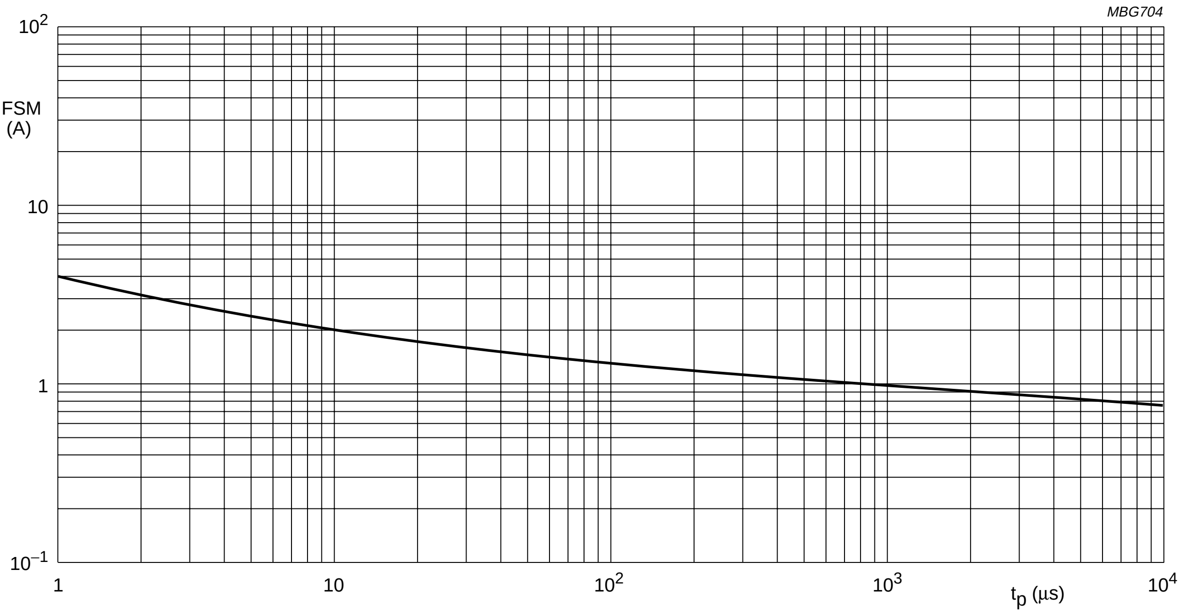
Device mounted on an FR4 printed-circuit board; lead length 10 mm.

Fig.2 Maximum permissible continuous forward current as a function of ambient temperature.



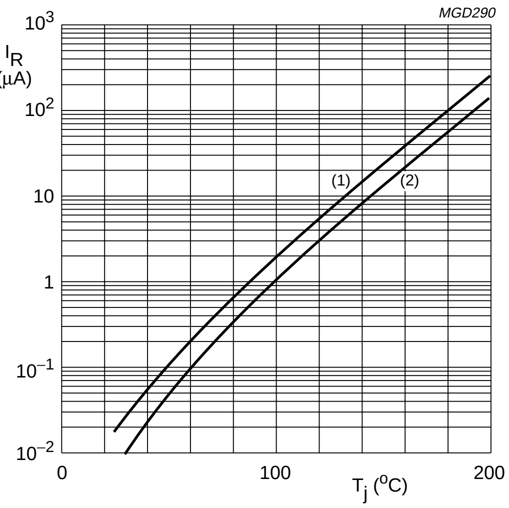
(1) T_j = 175 °C; typical values.
(2) T_j = 25 °C; typical values.
(3) T_j = 25 °C; maximum values.

Fig.3 Forward current as a function of forward voltage.



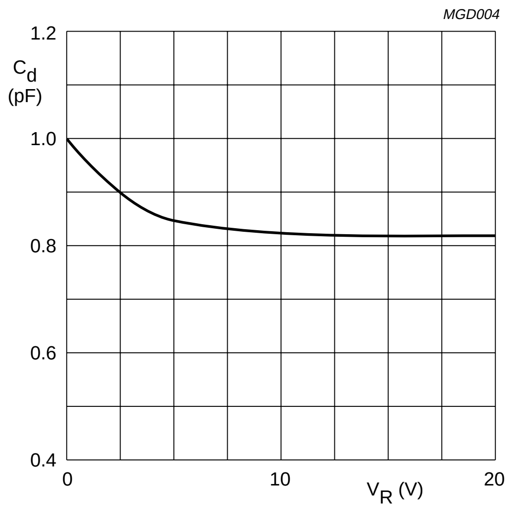
Based on square wave currents.
T_j = 25 °C prior to surge.

Fig.4 Maximum permissible non-repetitive peak forward current as a function of pulse duration.



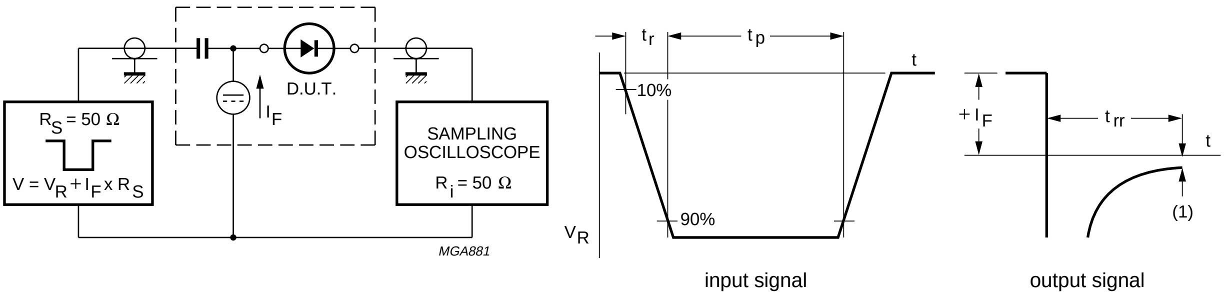
(1) V_R = 75 V; typical values.
(2) V_R = 20 V; typical values.

Fig.5 Reverse current as a function of junction temperature.



f = 1 MHz; T_j = 25 °C.

Fig.6 Diode capacitance as a function of reverse voltage; typical values.



(1) I_R = 1 mA.

Fig.7 Reverse recovery voltage test circuit and waveforms.

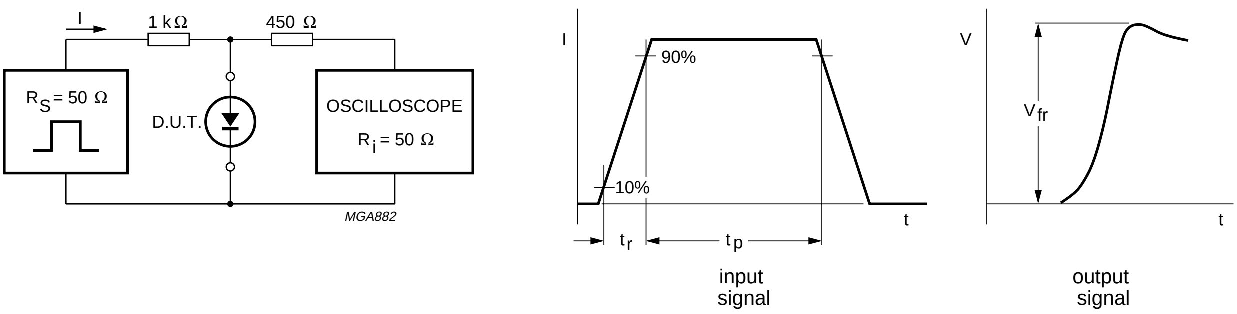
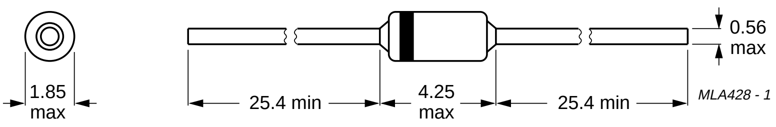


Fig.8 Forward recovery voltage test circuit and waveforms.

PACKAGE OUTLINE



Dimensions in mm.

Fig.9 SOD27 (DO-35).

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

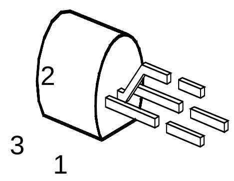
These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale

SIEMENS

PNP Silicon AF Transistors

BC 327
BC 328

- High current gain
- High collector current
- Low collector-emitter saturation voltage
- Complementary types: BC 337, BC 338 (NPN)



Type	**Marking**	**Ordering Code**	**Pin Configuration** 1	2	3	**Package**[1)]
BC 327	–	Q62702-C311	C	B	E	TO-92
BC 327-16		Q62702-C311-V3				
BC 327-25		Q62702-C311-V4				
BC 327-40		Q62702-C311-V2				
BC 328		Q62702-C312				
BC 328-16		Q62702-C312-V3				
BC 328-25		Q62702-C312-V4				
BC 328-40		Q62702-C312-V2				

1) For detailed information see chapter Package Outlines.

Maximum Ratings

Parameter	Symbol	Values BC 327	Values BC 328	Unit
Collector-emitter voltage	V_{CE0}	45	25	V
Collector-base voltage	V_{CB0}	50	30	
Emitter-base voltage	V_{EB0}	5		
Collector current	I_C	800		mA
Peak collector current	I_{CM}	1		A
Base current	I_B	100		mA
Peak base current	I_{BM}	200		
Total power dissipation, $T_C = 66$ ˚C	P_{tot}	625		mW
Junction temperature	T_j	150		˚C
Storage temperature range	T_{stg}	– 65 … + 150		

Thermal Resistance

Junction - ambient	$R_{th\ JA}$	≤ 200	K/W
Junction - case[1)]	$R_{th\ JC}$	≤ 135	

1) Mounted on Al heat sink 15 mm × 25 mm × 0.5 mm.

Electrical Characteristics
at T_A = 25 ˚C, unless otherwise specified.

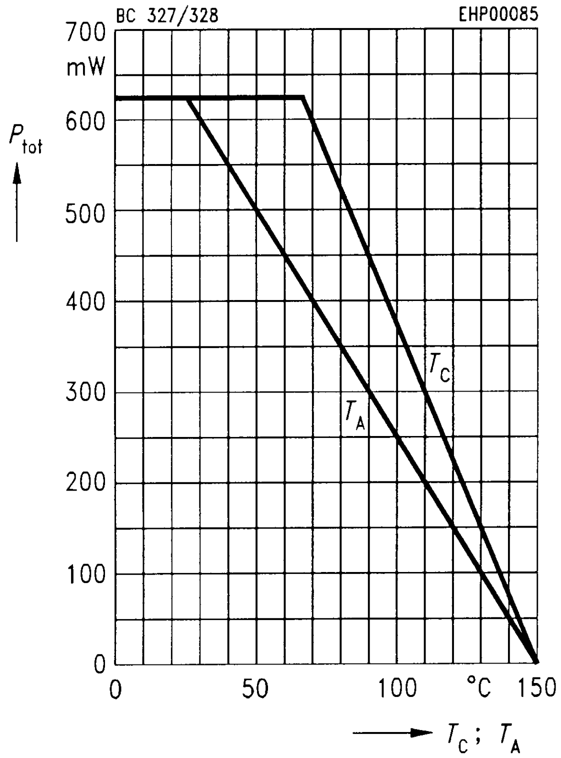
Parameter		Symbol	Values			Unit
			min.	typ.	max.	
DC characteristics						
Collector-emitter breakdown voltage I_C = 10 mA	BC 327 BC 328	$V_{(BR)CE0}$	45 25	– –	– –	V
Collector-base breakdown voltage I_C = 100 µA	BC 327 BC 328	$V_{(BR)CB0}$	50 30	– –	– –	
Emitter-base breakdown voltage I_E = 10 µA		$V_{(BR)EB0}$	5	–	–	
Collector cutoff current V_{CB} = 25 V V_{CB} = 45 V V_{CB} = 25 V, T_A = 150 ˚C V_{CB} = 45 V, T_A = 150 ˚C	 BC 328 BC 327 BC 328 BC 327	I_{CB0}	 – – – –	 – – – –	 100 100 10 10	 nA nA µA µA
Emitter cutoff current V_{EB} = 4 V		I_{EB0}	–	–	100	nA
DC current gain[1)] I_C = 100 mA; V_{CE} = 1 V I_C = 300 mA; V_{CE} = 1 V	 BC 327/16; BC 328/16 BC 327/25; BC 328/25 BC 327/40; BC 328/40 BC 327/16; BC 328/16 BC 327/25; BC 328/25 BC 327/40; BC 328/40	h_{FE}	 100 160 250 60 100 170	 160 250 350 – – –	 250 400 630 – – –	–
Collector-emitter saturation voltage[1)] I_C = 500 mA; I_B = 50 mA		V_{CEsat}	–	–	0.7	V
Base-emitter saturation voltage[1)] I_C = 500 mA; I_B = 50 mA		V_{BEsat}	–	–	2	

1) Pulse test: $t \leq 300$ µs, $D \leq 2$ %.

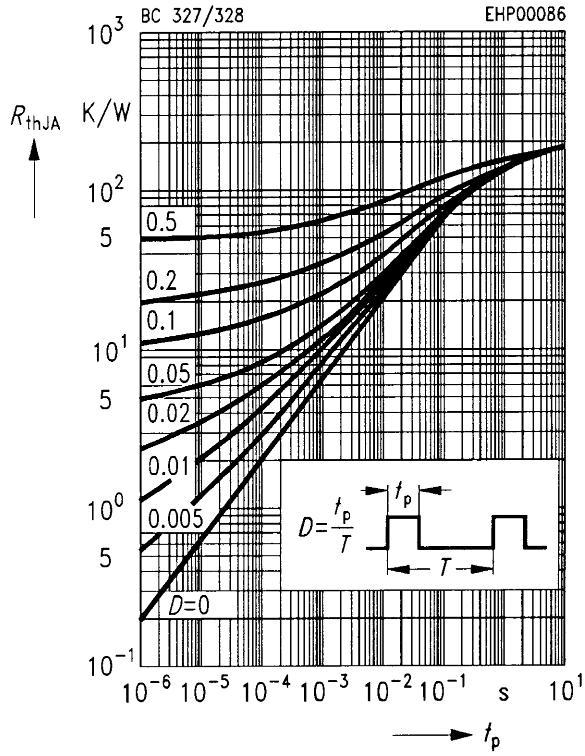
Electrical Characteristics
at T_A = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 20 MHz	f_T	–	200	–	MHz
Output capacitance V_{CB} = 10 V, f = 1 MHz	C_{obo}	–	12	–	pF
Input capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{ibo}	–	60	–	

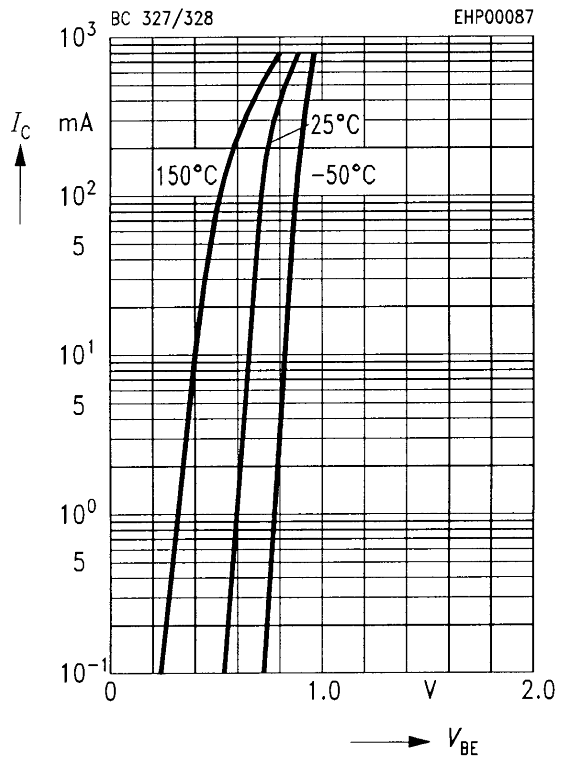
Total power dissipation $P_{tot} = f(T_A; T_C)$



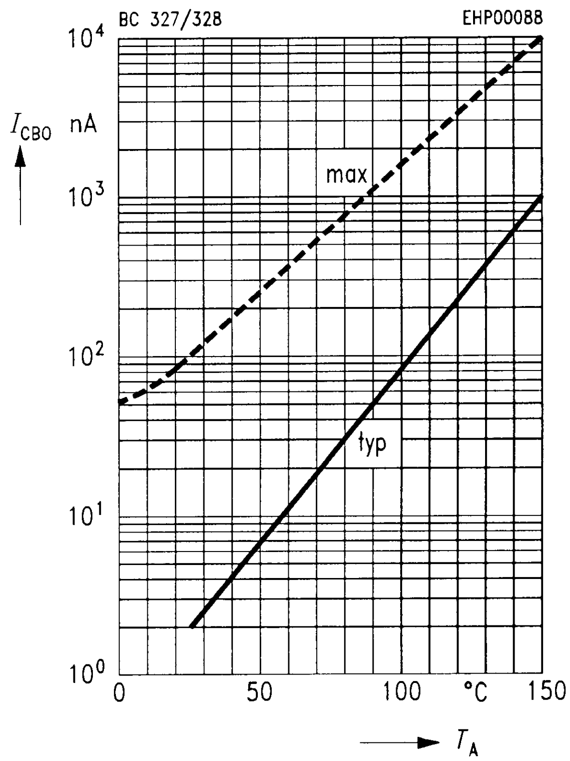
Permissible pulse load $R_{thJA} = f(t_p)$



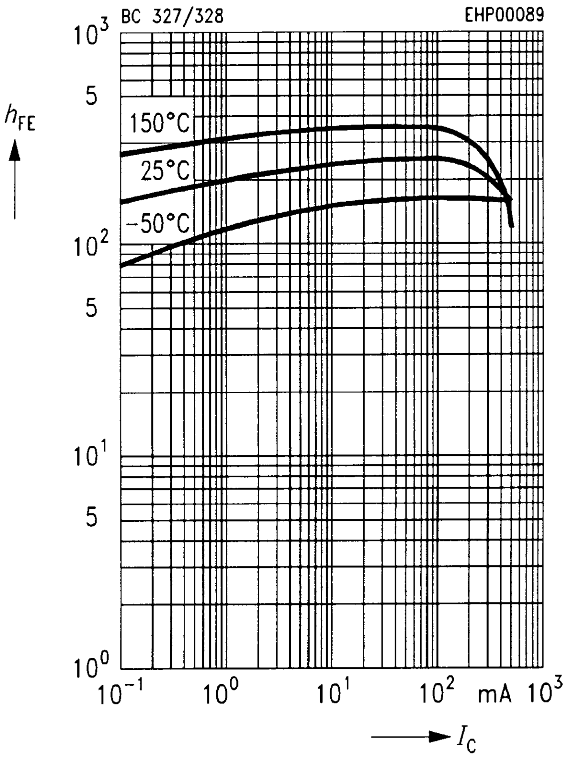
Collector current $I_C = f(V_{BE})$
V_{CE} = 1 V



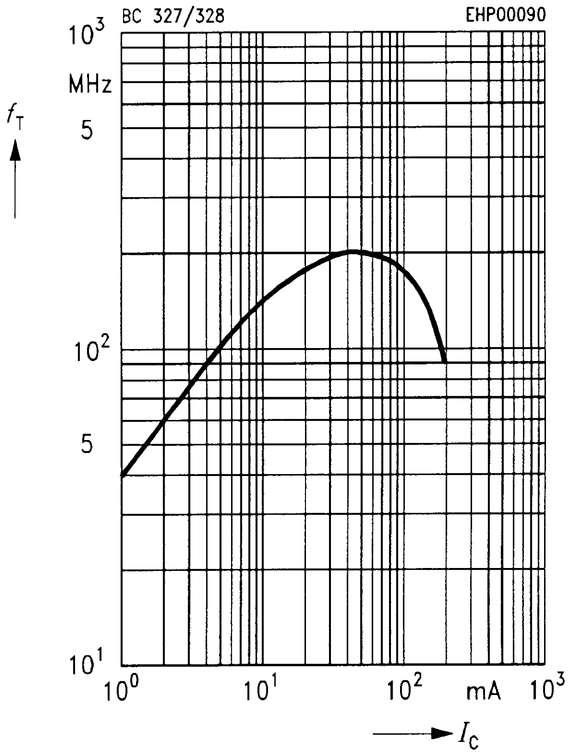
Collector cutoff current $I_{CB0} = f(T_A)$
V_{CB} = 45 V



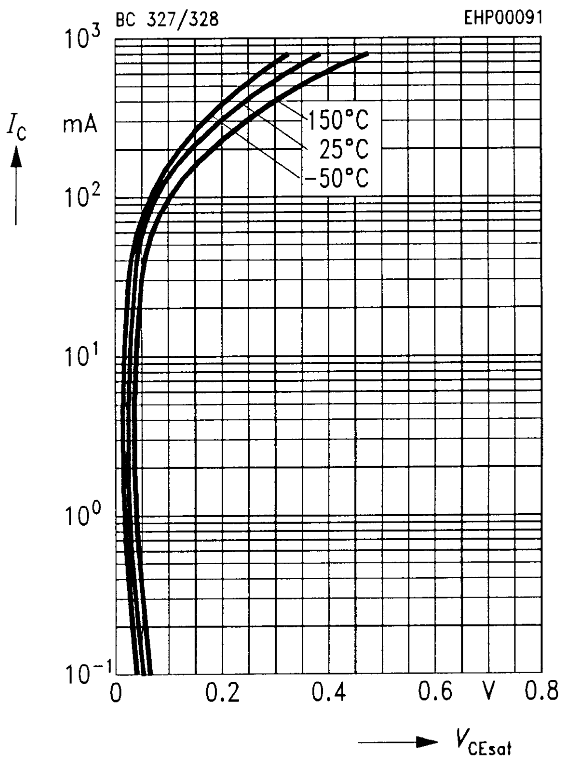
DC current gain $h_{FE} = f(I_C)$
$V_{CE} = 1$ V



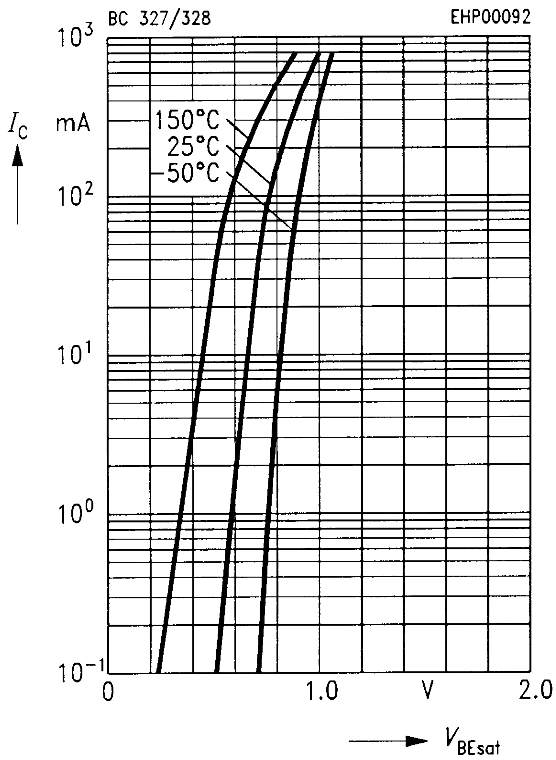
Transition frequency $f_T = f(I_C)$
f = 20 MHz, T_A = 25 ˚C



Collector-emitter saturation voltage
$V_{CEsat} = f(I_C)$
$h_{FE} = 10$



Base-emitter saturation voltage
$V_{BEsat} = f(I_C)$
$h_{FE} = 10$



OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

Log Amplifier

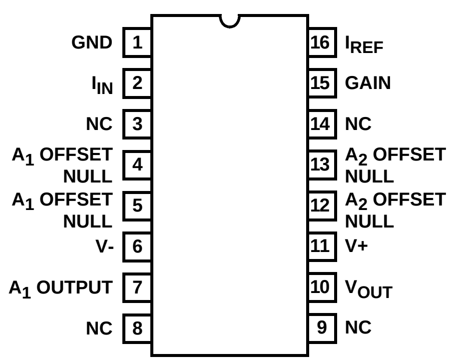
The ICL8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1V of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

Part Number Information

PART NUMBER	ERROR (25°C)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. NO.
ICL8048BCJE	30mV	0 to 70	16 Ld CERDIP	F16.3

Pinout

ICL8048 (CERDIP)
TOP VIEW

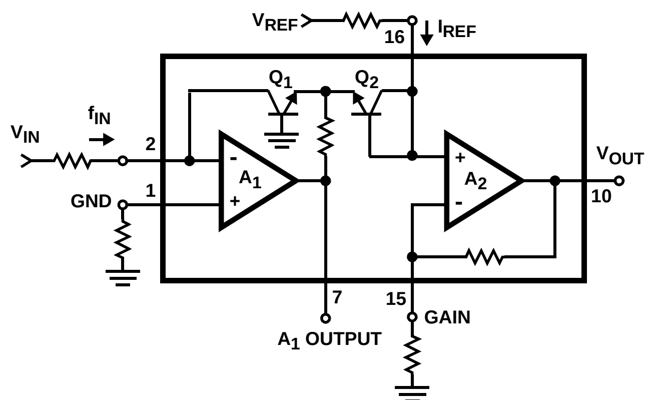


Features

- Full Scale Accuracy 0.5%
- Temperature Compensated Operation . . . . . . 0^oC to 70^oC
- Scale Factor, Adjustable 1V/Decade
- Dynamic Current Range. 120dB
- Dynamic Voltage Range 60dB
- Dual JFET Input Op Amps

Functional Diagram

ICL8048



Absolute Maximum Ratings

Supply Voltage . . . . ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage Between Offset Null and V+ . . . . ±0.5V
Output Short Circuit Duration. . . . . Indefinite

Operating Conditions

Temperature Range. . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package.	75	22

Maximum Junction Temperature (Hermetic Package or Die) . . . 175^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC

Die Characteristics

Number of Transistors or Gates 62

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_S = \pm15V$, $T_A = 25^oC$, $I_{REF} = 1mA$, Scale Factor Adjusted for 1V/Decade, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	ICL4048BC			UNITS
		MIN	TYP	MAX	
Dynamic Range					
I_{IN} (1nA - 1mA)	$R_{IN} = 10k\Omega$	120	-	-	dB
V_{IN} (10mV - 10V)		60	-	-	dB
Error, % of Full Scale	I_{IN} = 1nA to 1mA	-	0.20	0.5	%
	$T_A = 0^oC$ to 70^oC, I_{IN} = 1nA to 1mA	-	0.60	1.25	%
Error, Absolute Value	I_{IN} = 1nA to 1mA	-	12	30	mV
	$T_A = 0^oC$ to 70^oC, I_{IN} = 1nA to 1mA	-	36	75	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1nA to 1mA	-	0.8	-	mV/^oC
Power Supply Rejection Ratio	Referred to Output	-	2.5	-	mV/V
Offset Voltage (A_1 and A_2)	Before Nulling	-	15	25	mV
Wideband Noise	At Output, for $I_{IN} = 100\mu A$	-	250	-	μV_{RMS}
Output Voltage Swing	$R_L = 10k\Omega$	±12	±14	-	V
	$R_L = 2k\Omega$	±10	±13	-	V
Power Consumption		-	150	200	mW
Supply Current		-	5	6.7	mA

Typical Performance Curves

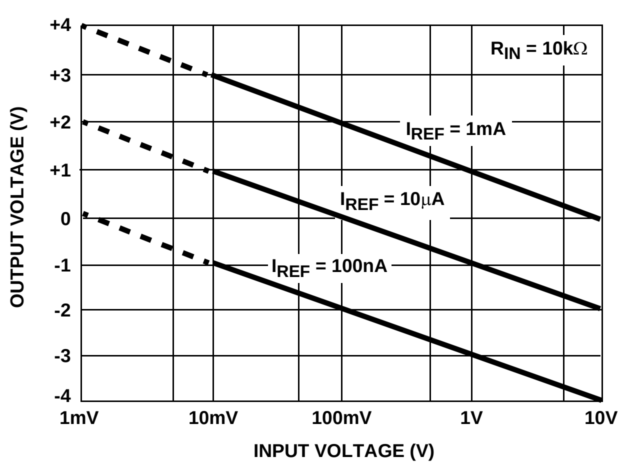


FIGURE 1. TRANSFER FUNCTION FOR VOLTAGE INPUTS

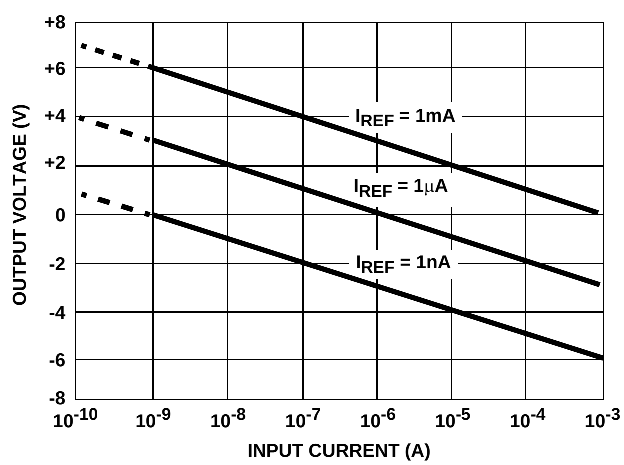


FIGURE 2. TRANSFER FUNCTION FOR CURRENT INPUTS

Typical Performance Curves (Continued)

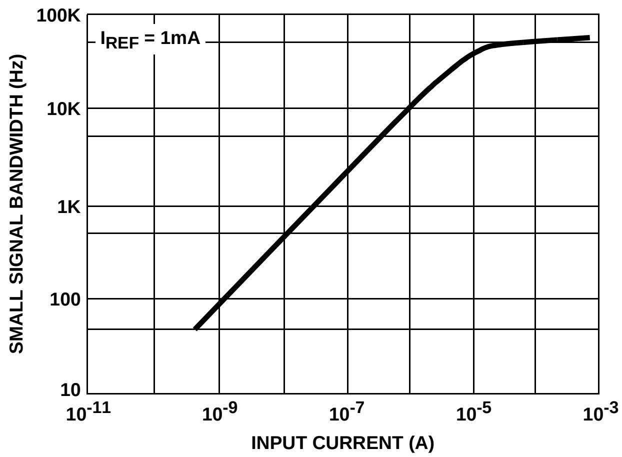


FIGURE 3. SMALL SIGNAL BANDWIDTH vs INPUT CURRENT

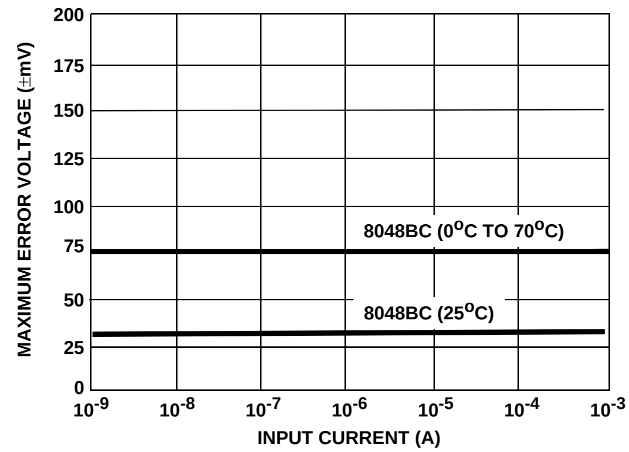


FIGURE 4. MAXIMUM ERROR VOLTAGE AT THE OUTPUT vs INPUT CURRENT

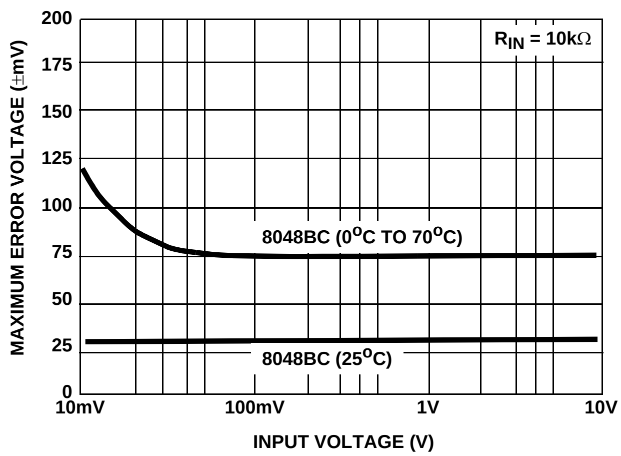


FIGURE 5. MAXIMUM ERROR VOLTAGE AT THE OUTPUT vs INPUT VOLTAGE

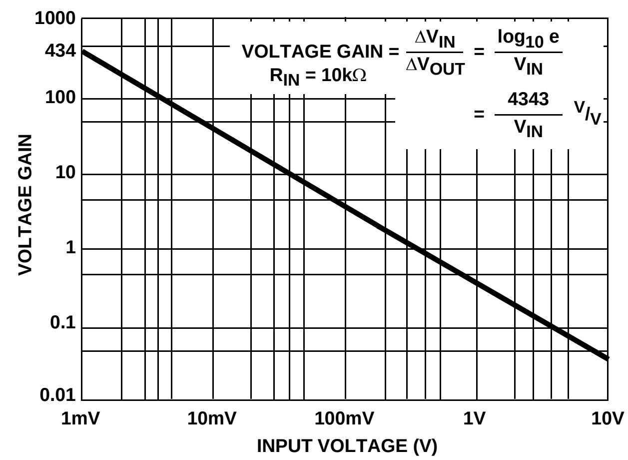


FIGURE 6. SMALL SIGNAL VOLTAGE GAIN vs INPUT VOLTAGE FOR R_S = 10kΩ

ICL8048 Detailed Description

The ICL8048 relies for its operation on the well known exponential relationship between the collector current and the base emitter voltage of a transistor:

$$I_C = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] \quad \text{(EQ. 1)}$$

For base emitter voltages greater than 100mV, Equation 1 becomes

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right) \quad \text{(EQ. 2)}$$

From Equation 2, it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q}\log_{10}\left[\frac{I_{C1}}{I_{C2}}\right] \quad \text{(EQ. 3)}$$

Referring to Figure 7 it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1 + R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad \text{(EQ. 4)}$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25^oC; thus in order to generate 1V/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25^oC, and its temperature coefficient is

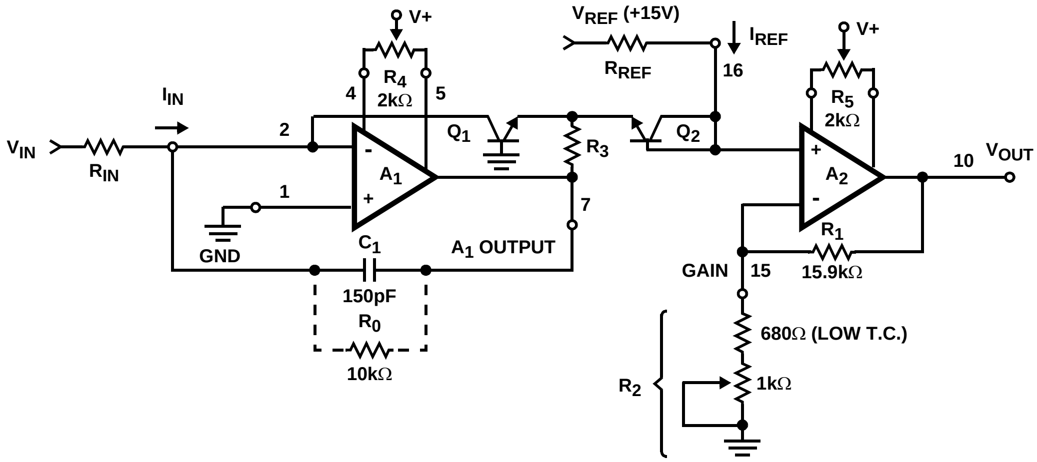


FIGURE 7. ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1V/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

ICL8048 Offset and Scale Factor Adjustment

A log amp, unlike an op amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 7, this is done as follows:

1. Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current source inputs.
2. Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.
3. Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for $V_{OUT} = 3V$ (for a 1V/decade scale factor) or 6V (for a 2V/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the ICL8048 is to be used for inputs which only span the range 100µA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

Applications Information

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048, are primarily directed towards setting up 1V (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \qquad \text{(EQ. 5)}$$

By adjusting R_2 (Figure 7) the scale factor "K" in Equation 5 can be varied. The effect of changing K is shown graphically in Figure 8 for the log amp. The nominal value of R_2 required to give a specific value of K can be determined from Equation 6. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - 0.059)}\Omega \qquad \text{(EQ. 6)}$$

ICL8048 Automatic Offset Nulling Circuit

The ICL8048 is fundamentally a logarithmic current amplifier. It can be made to act as a voltage amplifier by placing a resistor between the current input and the voltage source but, since $I_{IN} = (V_{IN} - V_{OFFSET})/R_{IN}$, this conversion is accurate only when V_{IN} is much greater than the offset voltage. A substantial reduction of V_{OFFSET} would allow voltage operation over a 120dB range.

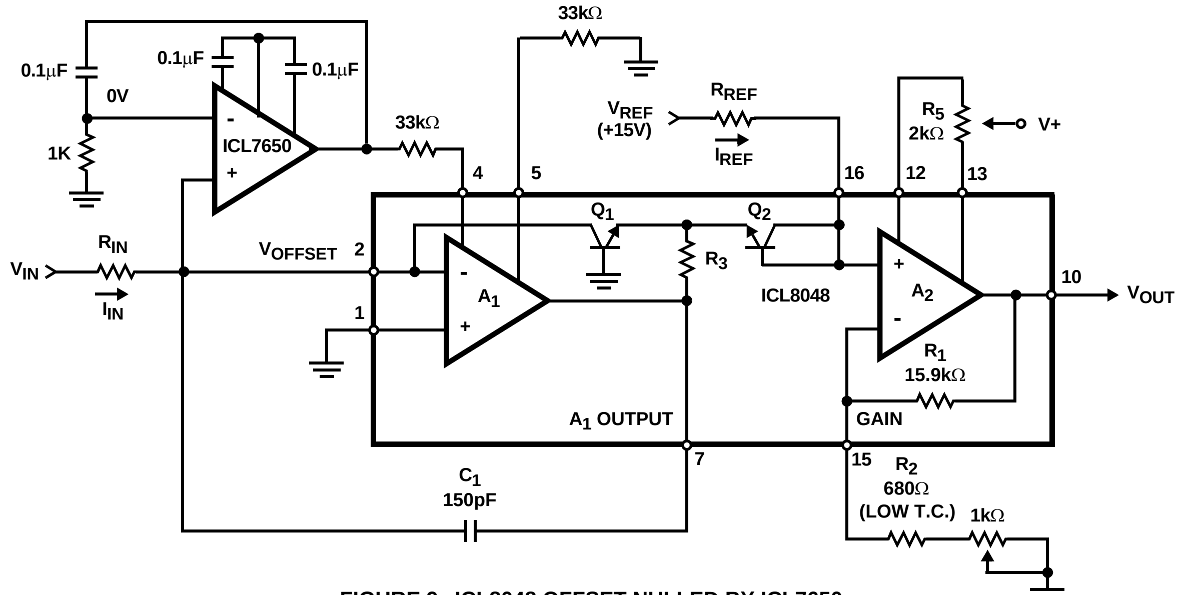


FIGURE 9. ICL8048 OFFSET NULLED BY ICL7650

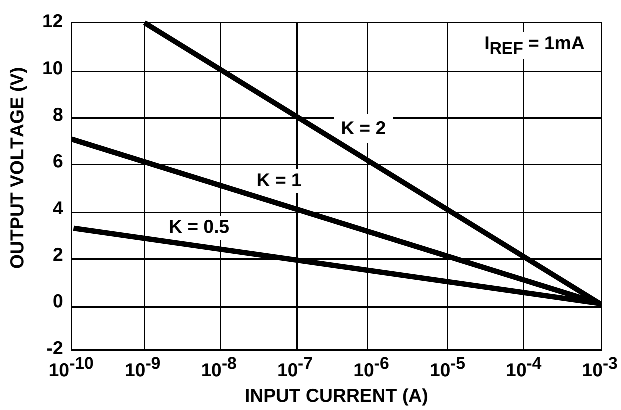


FIGURE 8. EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

Figure 9 shows the ICL8048 in an automatic offset nulling configuration using the ICL7650S. The extremely low offset voltage of the ICL7650S forces its non-inverting input (and thus pin 2 of the ICL8048) to the same potential as its inverting input by nulling the first stage of the log amp. Since V_{OFFSET} is now within a few μV of ground potential, R_{IN} can perform its voltage to current conversion much more accurately, and without an offset trimmer pot. Step 1 of the offset and scale factor adjustment is eliminated, simplifying calibration.

NOTE: The ICL7650S op amp has a maximum supply voltage of 18V. The ICL8048 will operate at this voltage, but I_{REF} must be limited to 200μA or less for proper calibration and operation. Best performance will be achieved when the ICL7650S has a ±3V to ±8V supply and the ICL8048 is at its recommended ±15V supply. See A053 for a method of powering the ICL7650S from a ±15V source.

Frequency Compensation

Although the op amps in the ICL8048 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the ICL8048, 150pF should be connected between Pins 2 and 7 (Figure 7).

Error Analysis

Performing a meaningful error analysis of a circuit containing a log and antilog amplifiers is more complex than dealing with a similar circuit involving only op amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Curves section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 10.

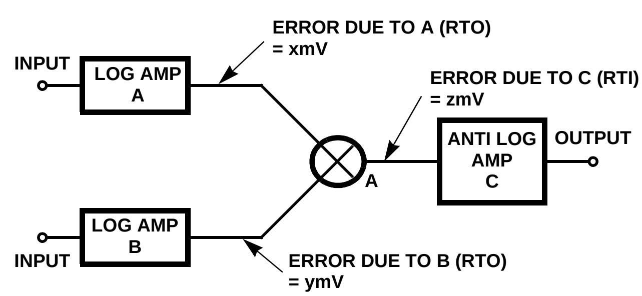


FIGURE 10.

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the-squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2}\ \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25^{o}C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 11 illustrates this point.

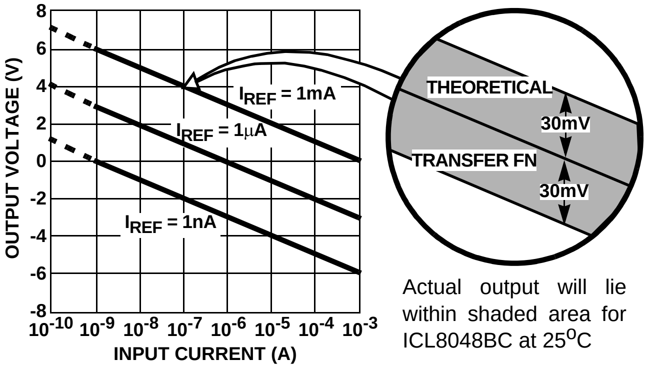


FIGURE 11. TRANSFER FUNCTION FOR CURRENT INPUTS

To determine the maximum error over the operating temperature range, the 0^{o}C to 70^{o}C absolute error values given in the table of electrical specifications should be used. For intermediate temperatures, assume a linear increase in the error between the 25^{o}C value and the 70^{o}C value.

It is important to note that the ICL8048 requires positive values of I_{REF}, and the input current must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

Setting Up the Reference Current

The input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 7). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 12.

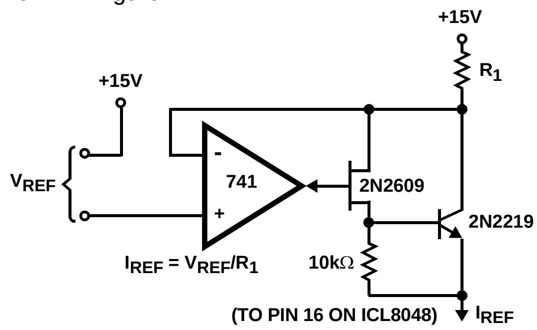


FIGURE 12.

Log of Ratio Circuit, Division

The ICL8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by Equation 7:

$$V_{OUT} = -K\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad \text{(EQ. 7)}$$

Clearly it is possible to perform division using just one ICL8048, followed by an antilog amplifier. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 12 is again recommended if the I_{REF} input is to be modulated.

Definition of Terms

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

Dynamic Range. The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate.

Error, Absolute Value. The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage.

The absolute error specification is guaranteed over the dynamic range.

± 10 Volt Precision Reference Series

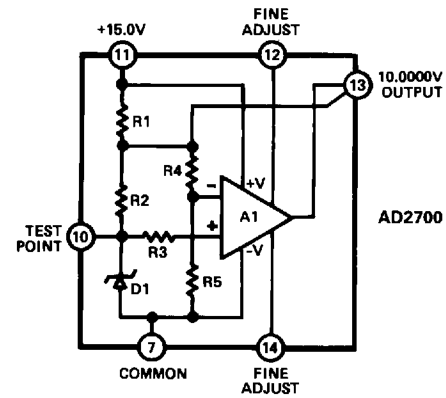
AD2700/AD2701/AD2702

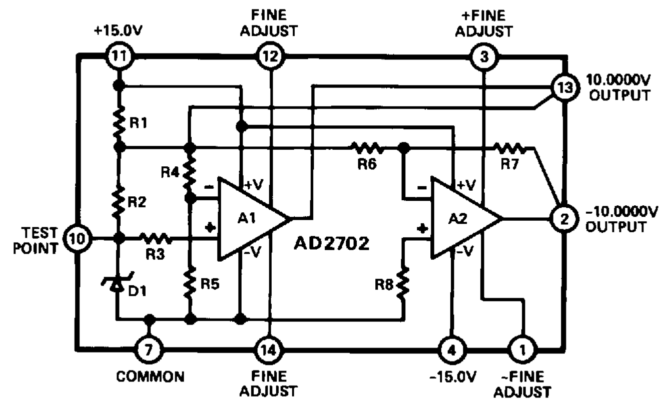
ANALOG DEVICES

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed −55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected
Available as /883B

FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require −10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from −25°C to +85°C and "S" and "U" grades for the −55°C to +125°C temperature range. Screening to MIL-STD-883 is available for "S" and "U" grades of the AD2700 family.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	−10.000V
AD2702	±10.000V

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel: 617/329-4700 Twx: 710/394-6577
Telex: 924491 Cables: ANALOG NORWOODMASS

AD2700/AD2701/AD2702—SPECIFICATIONS (max or min @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted.)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	*	**
AD2701 -10.000V	±0.005V	±0.0025V	*	**
AD2702 ±10.000V	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust (typ)	*	*	*
PACKAGE OPTION[3,4]	DH-14C	DH-14C	DH-14C	DH-14C

NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

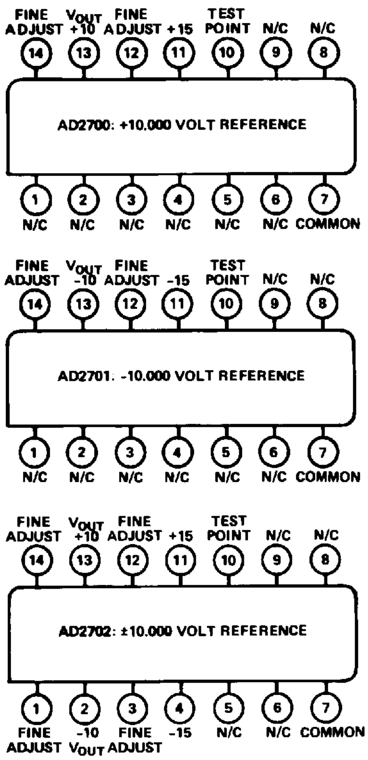
[1] Specified with resistive load to common. Device not intended for use in driving a dynamic load.

[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.

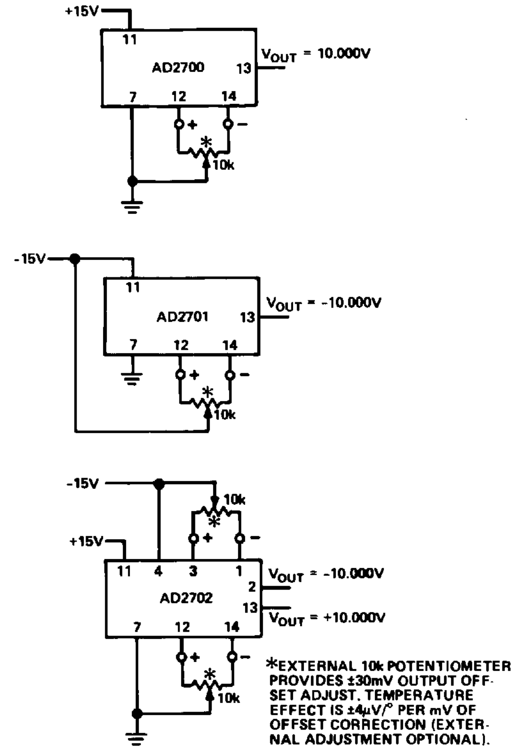
[3] Analog Devices reserves the right to ship side-brazed ceramic packages (outline DH-14D) in lieu of the standard ceramic packages for J and L grade parts."

[4] See Section 14 for package outline information.

Specifications subject to change without notice.



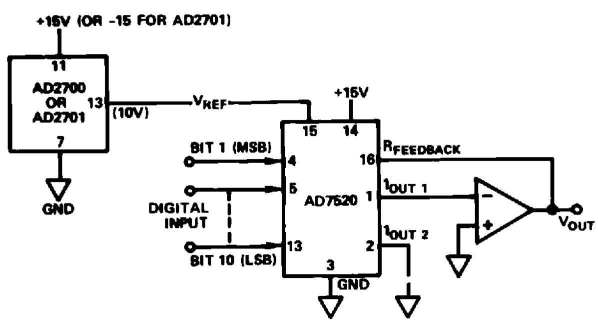
Pin Designations



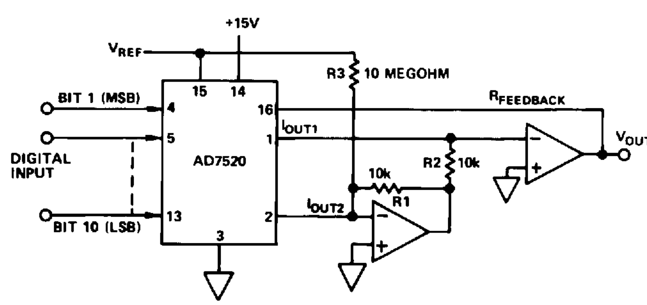
Fine Trim Connections

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to −10 volt output range. Alternatively, using the −10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of −10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.



Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = $2^{-10}\ V_{REF}$

Table I. Code Table – Unipolar Binary Operation

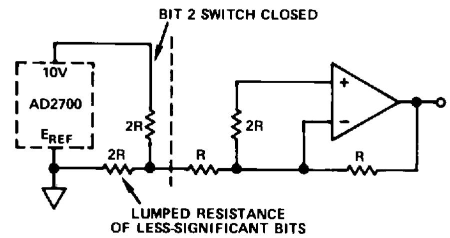
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9}\ V_{REF}$

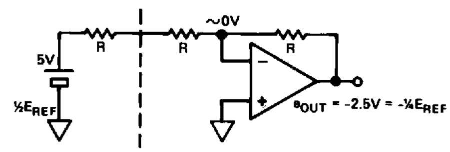
Table II. Code Table – Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

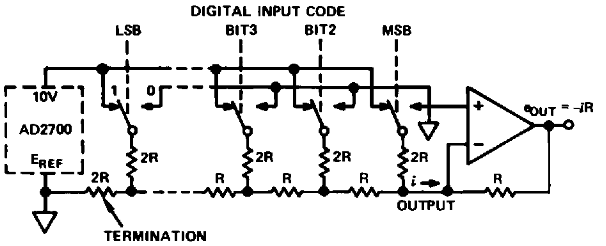
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $½(-R/2R)E_{REF} = ¼E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence – because the amplifier summing point is at virtual ground – the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



b. Example: Contribution of Bit 2; All Other Bits "0"



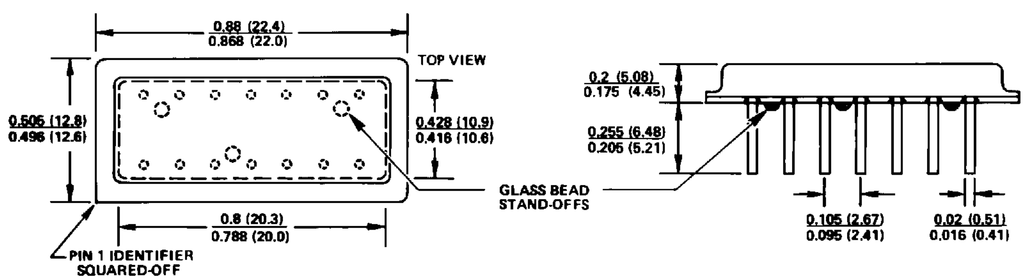
c. Simplified Equivalent of Circuit (b.)



a. Basic Circuit

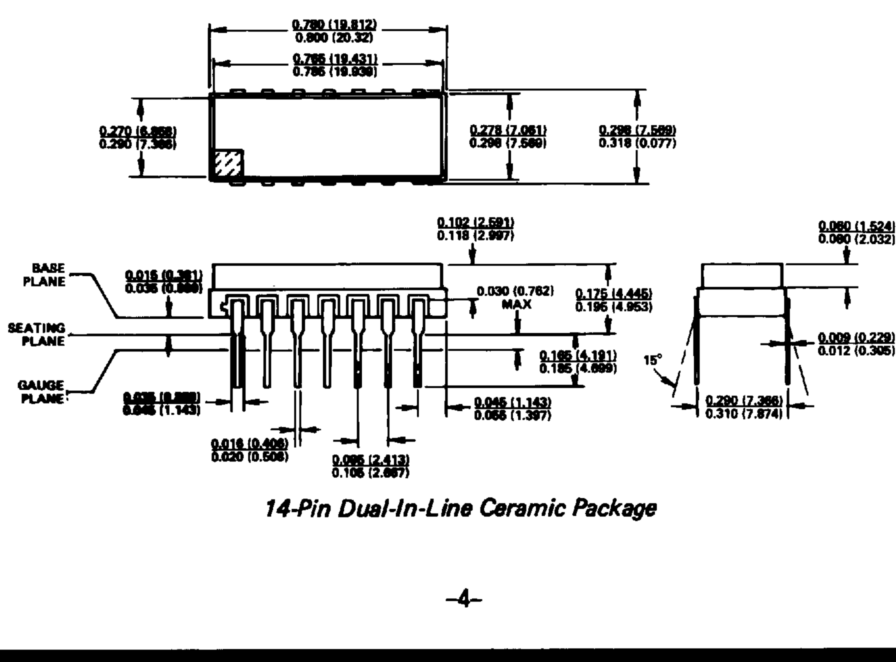
PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).



Hermetically sealed 14-Pin Dual-In-Line (Gross leak tested per MIL-STD-883, Method 1014)
Pin 7 is electrically connected to the case. Case has metal bottom surface.

14-Pin Dual-In-Line Metal Package



14-Pin Dual-In-Line Ceramic Package

C350a–8–8/83

PRINTED IN U.S.A.

National Semiconductor

April 1998

LM109/LM309
5-Volt Regulator

General Description

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

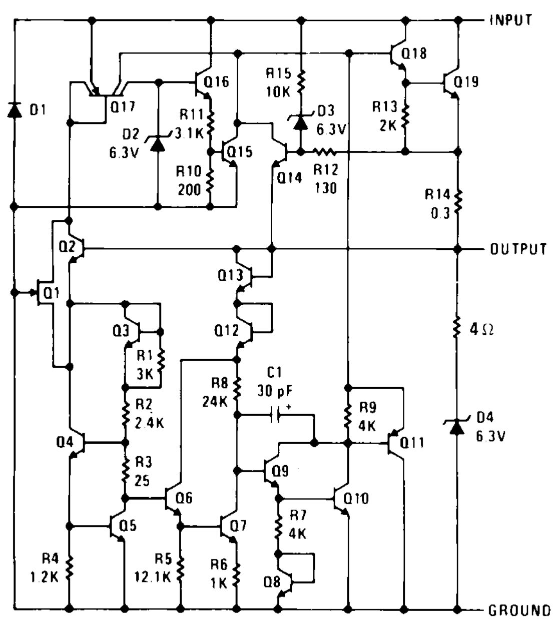
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Features

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

Schematic Diagram



DS007138-1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	−55˚C to +150˚C
LM309	0˚C to +125˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	300˚C

Electrical Characteristics (Note 2)

Parameter	Conditions	LM109			LM309			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	T_j = 25˚C	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	T_j = 25˚C 7.10V ≤ V_{IN} ≤ 25V		4.0	50		4.0	50	mV
Load Regulation	T_j = 25˚C							
TO-39 Package	5 mA ≤ I_{OUT} ≤ 0.5A		15	50		15	50	mV
TO-3 Package	5 mA ≤ I_{OUT} ≤ 1.5A		15	100		15	100	mV
Output Voltage	7.40V ≤ V_{IN} ≤ 25V, 5 mA ≤ I_{OUT} ≤ I_{MAX}, P < P_{MAX}	4.6		5.4	4.75		5.25	V
Quiescent Current	7.40V ≤ V_{IN} ≤ 25V		5.2	10		5.2	10	mA
Quiescent Current Change	7.40V ≤ V_{IN} ≤ 25V			0.5			0.5	mA
	5 mA ≤ I_{OUT} ≤ I_{MAX}			0.8			0.8	mA
Output Noise Voltage	T_A = 25˚C 10 Hz ≤ f ≤ 100 kHz		40			40		µV
Long Term Stability			10			20		mV
Ripple Rejection	T_j = 25˚C	50			50			dB
Thermal Resistance, Junction to Case	(Note 3)							
TO-39 Package			15			15		˚C/W
TO-3 Package			2.5			2.5		˚C/W

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

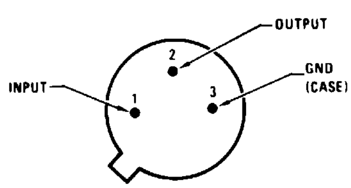
Note 2: Unless otherwise specified, these specifications apply −55˚C ≤ T_j ≤ +150˚C for the LM109 and 0˚C ≤ T_j ≤ +125˚C for the LM309; V_{IN} = 10V; and I_{OUT} = 0.1A for the TO-39 package or I_{OUT} = 0.5A for the TO-3 package. For the TO-39 package, I_{MAX} = 0.2A and P_{MAX} = 2.0W. For the TO-3 package, I_{MAX} = 1.0A and P_{MAX} = 20W.

Note 3: Without a heat sink, the thermal resistance of the TO-39 package is about 150˚C/W, while that of the TO-3 package is approximately 35˚C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

Note 4: Refer to RETS109H drawing for LM109H or RETS109K drawing for LM109K military specifications.

Connection Diagrams

Metal Can Packages



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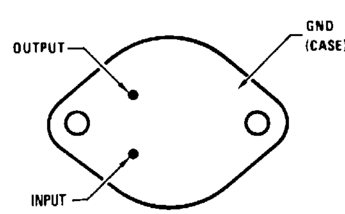
Order Number LM109H, LM109H/883 or LM309H
See NS Package Number H03A



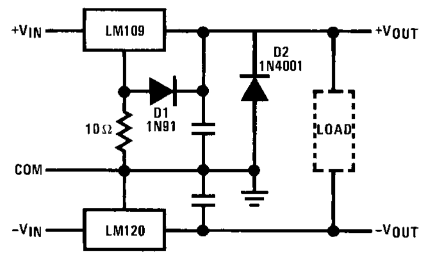
DS007138-34

Order Number LM109K STEEL or LM309K STEEL
See NS Package Number K02A
Order Number LM109K/883
See NS Package Number K02C

Application Hints

1. **Bypass the input** of the LM109 to ground with ≥ 0.2 µF ceramic or solid tantalum capacitor if main filter capacitor is more than 4 inches away.
2. **Avoid insertion of regulator into “live” socket** if input voltage is greater than 10V. The output will rise to within 2V of the unregulated input if the ground pin does not make contact, possibly damaging the load. The LM109 may also be damaged if a large output capacitor is charged up, then discharged through the internal clamp zener when the ground pin makes contact.
3. **The output clamp zener** is designed to absorb transients only. It will not clamp the output effectively if a failure occurs in the internal power transistor structure. Zener dynamic impedance is ≈ 4Ω. Continuous RMS current into the zener should not exceed 0.5A.
4. **Paralleling of LM109s** for higher output current is not recommended. Current sharing will be almost nonexistent, leading to a current limit mode operation for devices with the highest initial output voltage. The current limit devices may also heat up to the thermal shutdown point (≈ 175˚C). Long term reliability cannot be guaranteed under these conditions.
5. **Preventing latchoff** for loads connected to negative voltage:

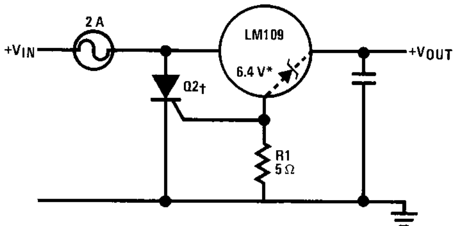
If the output of the LM109 is pulled negative by a high current supply so that the output pin is more than 0.5V negative with respect to the ground pin, the LM109 can latch off. This can be prevented by clamping the ground pin to the output pin with a germanium or Schottky diode as shown. A silicon diode (1N4001) at the output is also needed to keep the positive output from being pulled too far negative. The 10Ω resistor will raise $+V_{OUT}$ by ≈ 0.05V.



DS007138-7

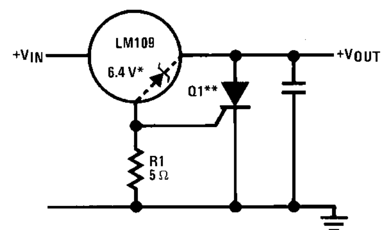
Crowbar Overvoltage Protection

Input Crowbar



DS007138-8

Output Crowbar



DS007138-9

*Zener is internal to LM109.

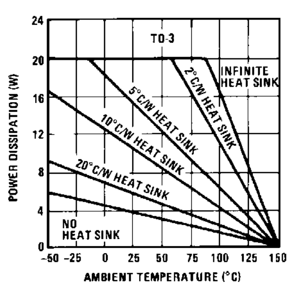
**Q1 must be able to withstand 7A continuous current if fusing is not used at regulator input. LM109 bond wires will fuse at currents above 7A.

†Q2 is selected for surge capability. Consideration must be given to filter capacitor size, transformer impedance, and fuse blowing time.

††Trip point is ≈ 7.5V.

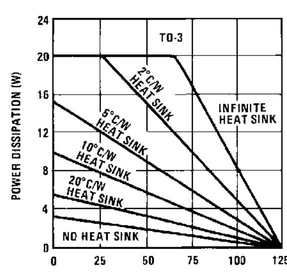
Typical Performance Characteristics

Maximum Average Power Dissipation (LM109K)



DS007138-16

Maximum Average Power Dissipation (LM309K)



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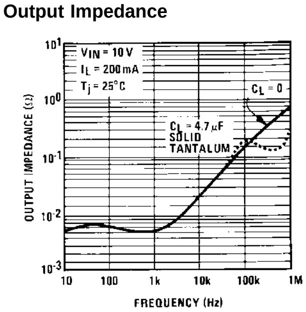
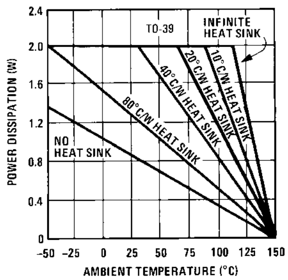
Output Impedance



DS007138-18

Typical Performance Characteristics (Continued)

Maximum Average Power Dissipation (LM109H)



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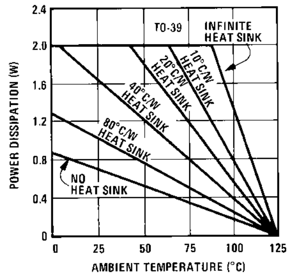
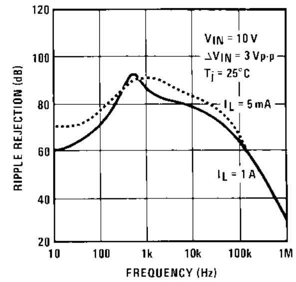
Maximum Average Power Dissipation (LM309H)



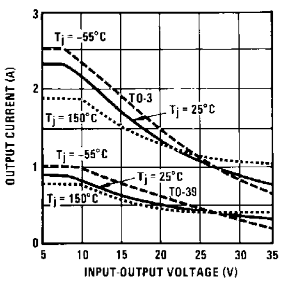
DS007138-20

Ripple Rejection



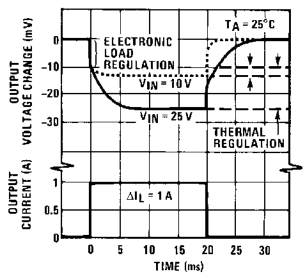
DS007138-21

Current Limit Characteristics (Note 5)



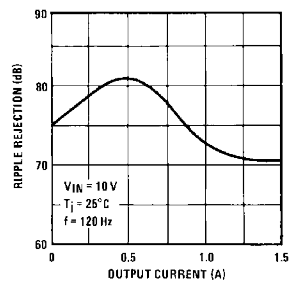
DS007138-22

Thermally Induced Output Voltage Variation



DS007138-23

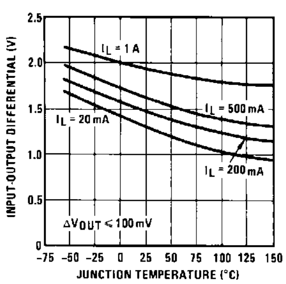
Ripple Rejection



DS007138-24

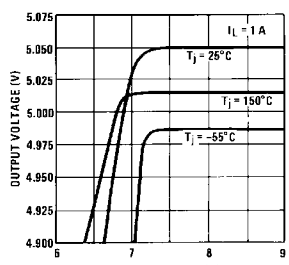
Note 5: Current limiting foldback characteristics are determined by input output differential, not by output voltage.

Input-Output Differential (V)



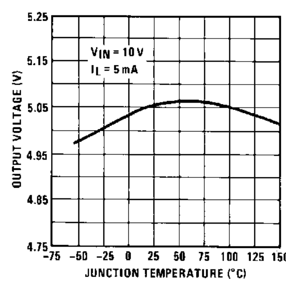
DS007138-25

Output Voltage (V)



DS007138-26

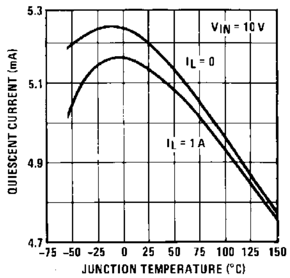
Output Voltage (V)



DS007138-27

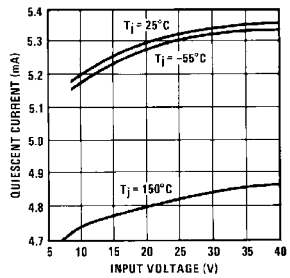
Typical Performance Characteristics (Continued)

Quiescent Current



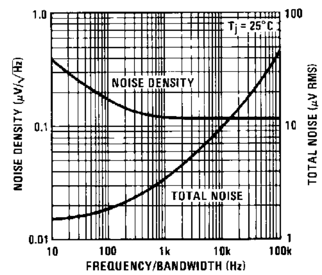
DS007138-28

Quiescent Current



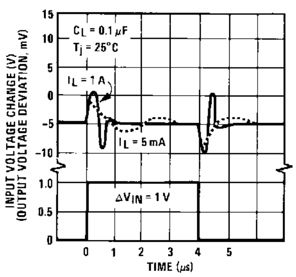
DS007138-29

Output Voltage Noise



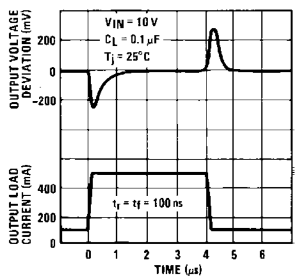
DS007138-30

Line Transient Response



DS007138-31

Load Transient Response



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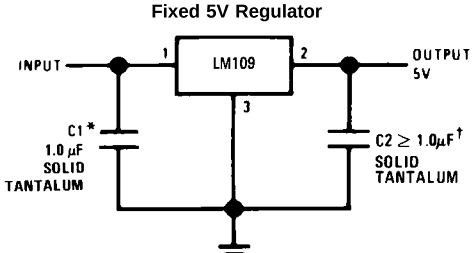
Typical Applications

Fixed 5V Regulator



DS007138-2

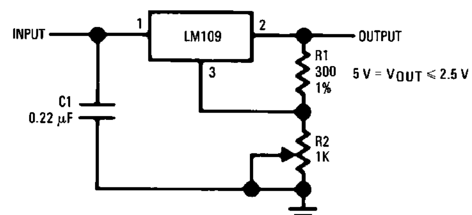
*Required if regulator is located more than 4" from power supply filter capacitor.

†Although no output capacitor is needed for stability, it does improve transient response.

C2 should be used whenever long wires are used to connect to the load, or when transient response is critical.

Note: Pin 3 electrically connected to case.

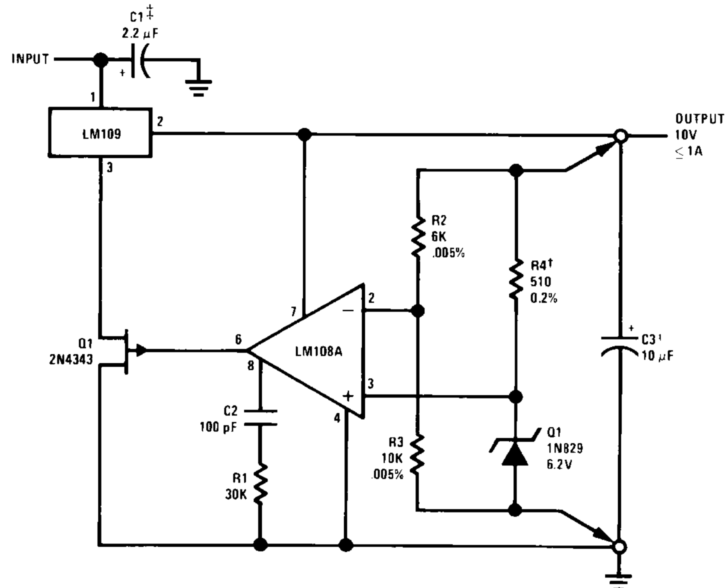
Adjustable Output Regulator



DS007138-4

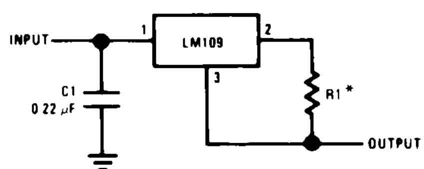
Typical Applications (Continued)

High Stability Regulator*



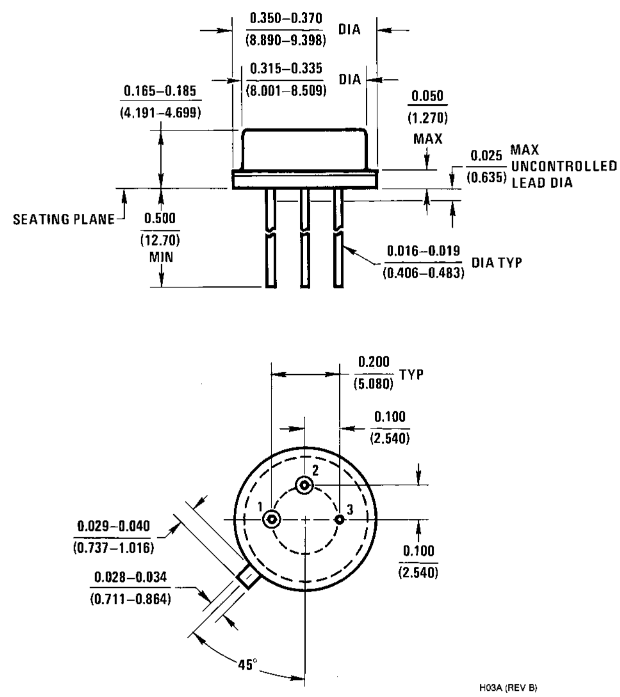
*Regulation better than 0.01%, load, line and temperature, can be obtained.
†Determines zener current. May be adjusted to minimize thermal drift.
‡Solid tantalum.

Current Regulator

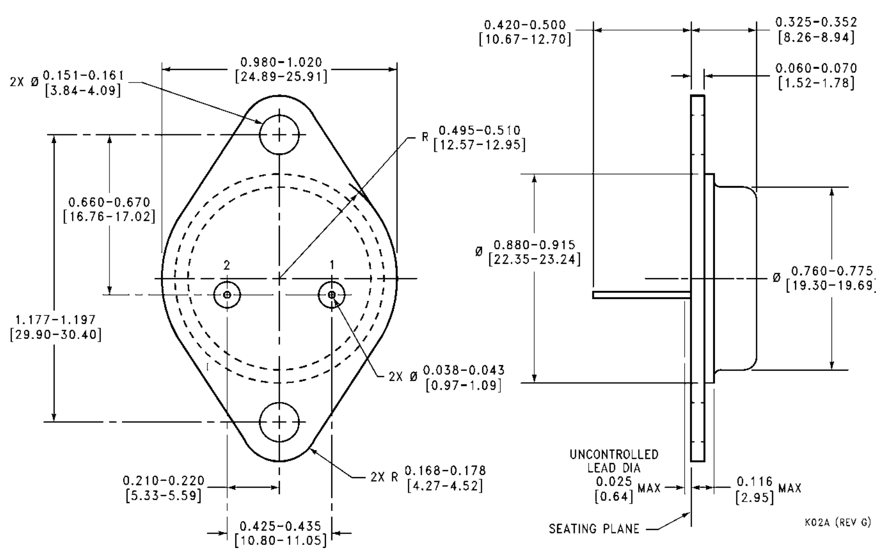


*Determines output current. If wirewound resistor is used, bypass with 0.1 µF.

Physical Dimensions inches (millimeters) unless otherwise noted

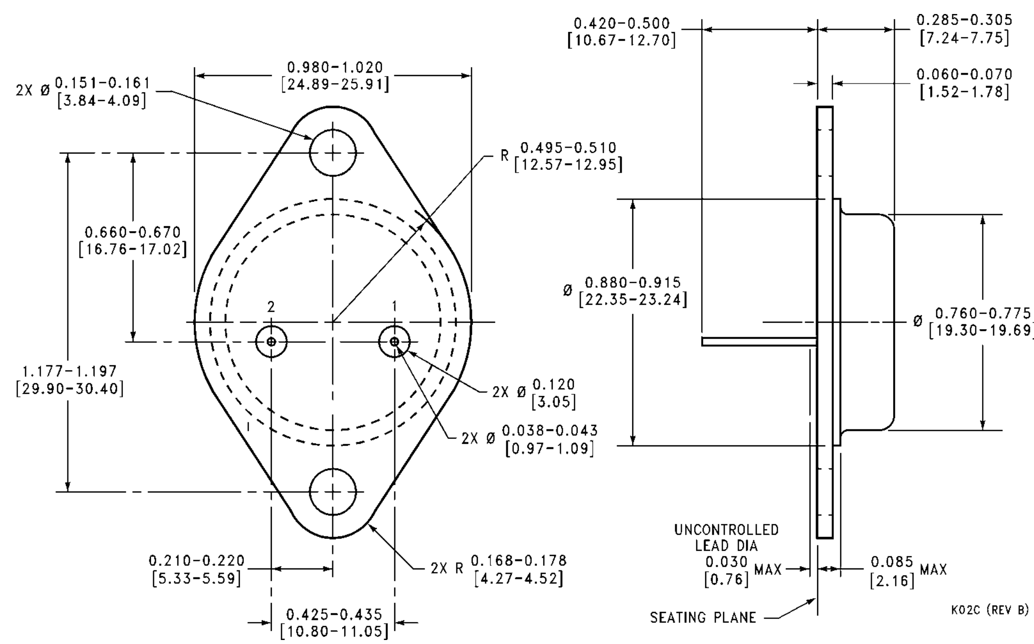


Metal Can Package (H)
Order Number LM109H, LM109H/883 or LM309H
NS Package Number H03A



Metal Can Package (K)
Order Number LM109K STEEL, LM309K STEEL
NS Package Number K02A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Metal Can Package (K)
Mil-Aero Product
Order Number LM109K/883
NS Package Number K02C

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Fax: 1-800-737-7018
Email: support@nsc.com

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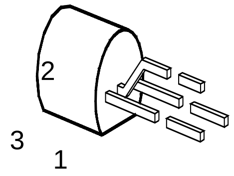
National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

SIEMENS

PNP Silicon AF Transistors

BC 327
BC 328

- High current gain
- High collector current
- Low collector-emitter saturation voltage
- Complementary types: BC 337, BC 338 (NPN)



Type	Marking	Ordering Code	Pin Configuration			Package[1)]
			1	**2**	**3**	
BC 327	–	Q62702-C311	C	B	E	TO-92
BC 327-16		Q62702-C311-V3				
BC 327-25		Q62702-C311-V4				
BC 327-40		Q62702-C311-V2				
BC 328		Q62702-C312				
BC 328-16		Q62702-C312-V3				
BC 328-25		Q62702-C312-V4				
BC 328-40		Q62702-C312-V2				

1) For detailed information see chapter Package Outlines.

Maximum Ratings

Parameter	Symbol	Values BC 327	BC 328	Unit
Collector-emitter voltage	V_{CE0}	45	25	V
Collector-base voltage	V_{CB0}	50	30	
Emitter-base voltage	V_{EB0}	5		
Collector current	I_C	800		mA
Peak collector current	I_{CM}	1		A
Base current	I_B	100		mA
Peak base current	I_{BM}	200		
Total power dissipation, $T_C = 66$ ˚C	P_{tot}	625		mW
Junction temperature	T_j	150		˚C
Storage temperature range	T_{stg}	– 65 … + 150		

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - ambient	$R_{th\ JA}$	≤ 200	K/W
Junction - case[1)]	$R_{th\ JC}$	≤ 135	

1) Mounted on Al heat sink 15 mm × 25 mm × 0.5 mm.

Electrical Characteristics
at T_A = 25 ˚C, unless otherwise specified.

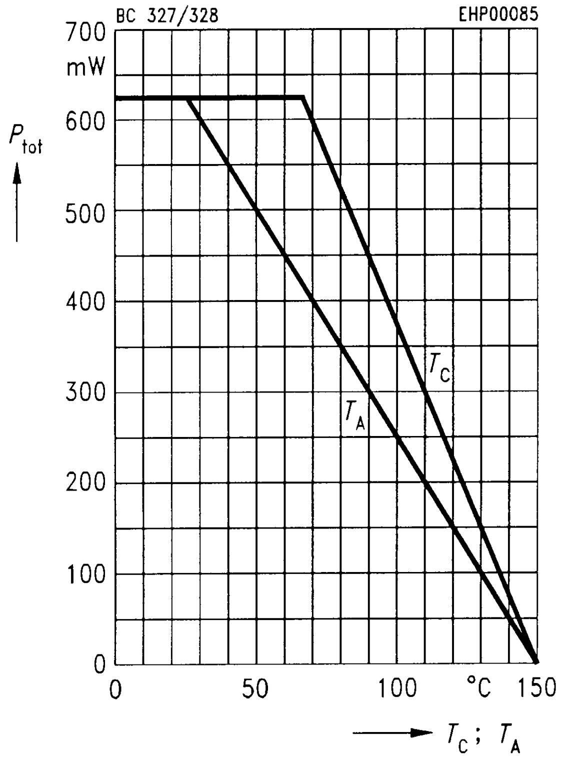
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Collector-emitter breakdown voltage I_C = 10 mA BC 327 BC 328	$V_{(BR)CE0}$	 45 25	 – –	 – –	V
Collector-base breakdown voltage I_C = 100 µA BC 327 BC 328	$V_{(BR)CB0}$	 50 30	 – –	 – –	
Emitter-base breakdown voltage I_E = 10 µA	$V_{(BR)EB0}$	5	–	–	
Collector cutoff current V_{CB} = 25 V BC 328 V_{CB} = 45 V BC 327 V_{CB} = 25 V, T_A = 150 ˚C BC 328 V_{CB} = 45 V, T_A = 150 ˚C BC 327	I_{CB0}	 – – – –	 – – – –	 100 100 10 10	 nA nA µA µA
Emitter cutoff current V_{EB} = 4 V	I_{EB0}	–	–	100	nA
DC current gain[1)] I_C = 100 mA; V_{CE} = 1 V BC 327/16; BC 328/16 BC 327/25; BC 328/25 BC 327/40; BC 328/40 I_C = 300 mA; V_{CE} = 1 V BC 327/16; BC 328/16 BC 327/25; BC 328/25 BC 327/40; BC 328/40	h_{FE}	 100 160 250 60 100 170	 160 250 350 – – –	 250 400 630 – – –	–
Collector-emitter saturation voltage[1)] I_C = 500 mA; I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base-emitter saturation voltage[1)] I_C = 500 mA; I_B = 50 mA	V_{BEsat}	–	–	2	

1) Pulse test: $t \leq 300$ µs, $D \leq 2$ %.

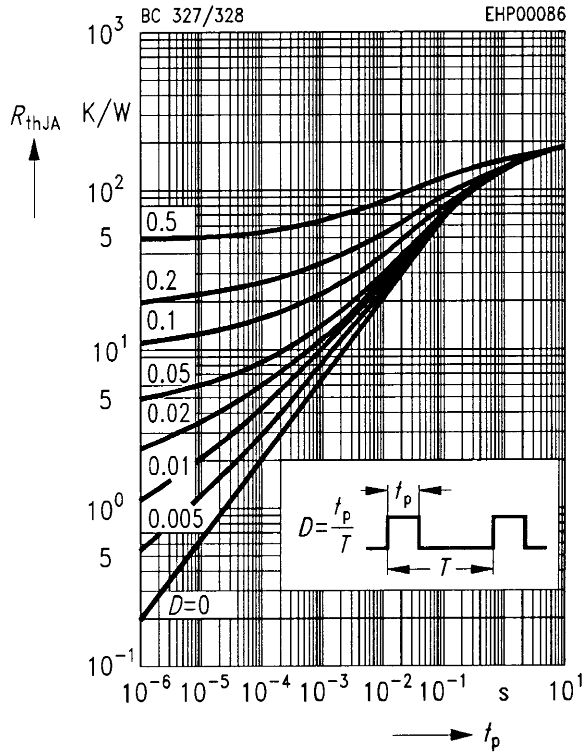
Electrical Characteristics
at T_A = 25 ˚C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 20 MHz	f_T	–	200	–	MHz
Output capacitance V_{CB} = 10 V, f = 1 MHz	C_{obo}	–	12	–	pF
Input capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{ibo}	–	60	–	

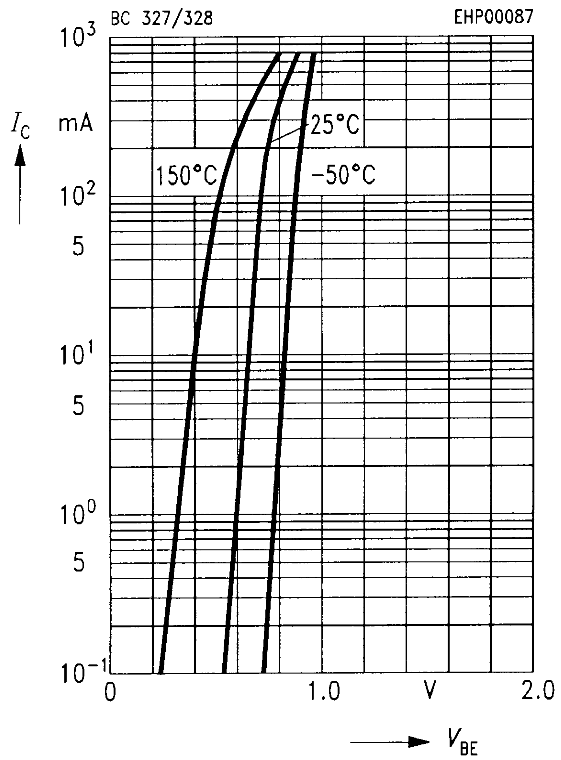
Total power dissipation $P_{tot} = f\,(T_A;\ T_C)$



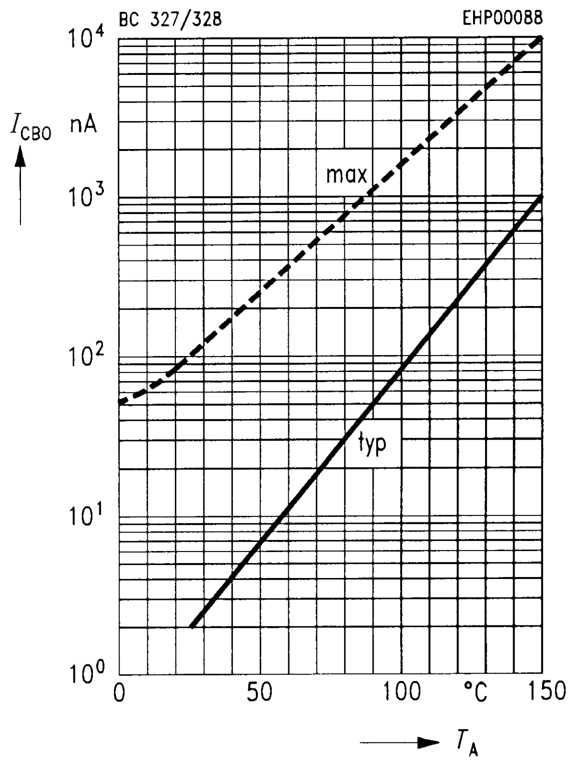
Permissible pulse load $R_{thJA} = f\,(t_p)$



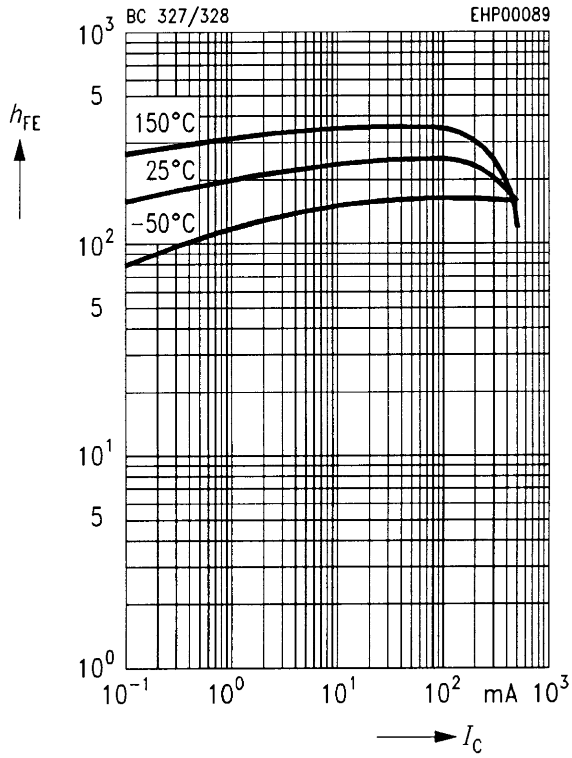
Collector current $I_C = f\,(V_{BE})$
V_{CE} = 1 V



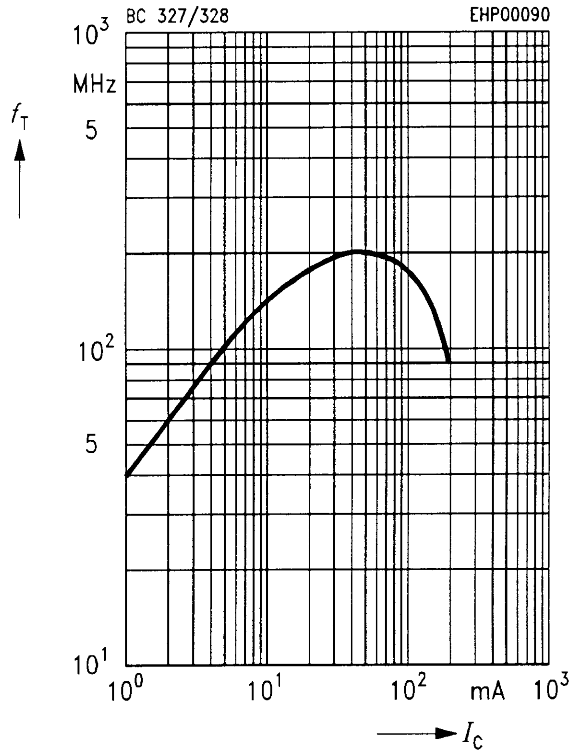
Collector cutoff current $I_{CB0} = f\,(T_A)$
V_{CB} = 45 V



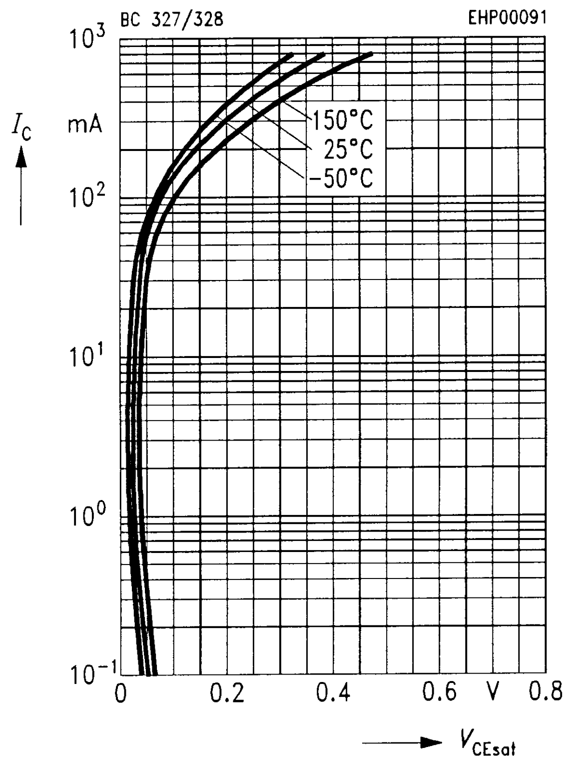
DC current gain $h_{FE} = f(I_C)$
V_{CE} = 1 V



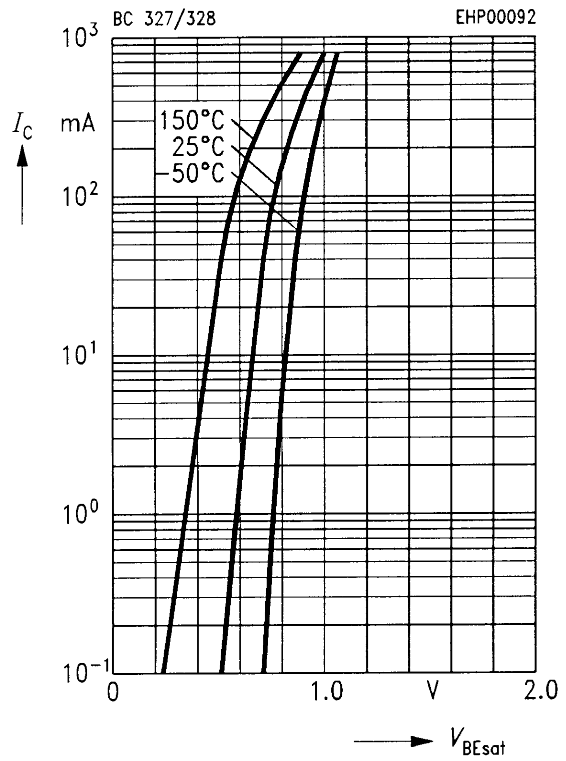
Transition frequency $f_T = f(I_C)$
f = 20 MHz, T_A = 25 ˚C



Collector-emitter saturation voltage
$V_{CEsat} = f(I_C)$
h_{FE} = 10



Base-emitter saturation voltage
$V_{BEsat} = f(I_C)$
h_{FE} = 10



LEHRBUCH

Peter F. Orlowski

Praktische Elektronik

Datenblätter
Analog- und CMOS-Technik

Springer Vieweg

Definition der Wechselspannungs-Parameter:

f_{MAX} Betriebsfrequenz. Dies ist die höchste Frequenz, bei der die Schaltung noch arbeitet.

t_{PHL} Übertragungsverzögerung vom Eingang zum Ausgang, wenn der Ausgang von H nach L geht.

t_{PLH} Übertragungsverzögerung vom Eingang zum Ausgang, wenn der Ausgang von L nach H geht.

t_{PZH} Freigabe-Verzögerungszeit. Sie wird zwischen Eingang und Ausgang gemessen, wenn der Ausgang vom Tristate-Zustand auf H wechselt.

t_{PZL} Freigabe-Verzögerungszeit. Sie wird zwischen Eingang und Ausgang gemessen, wenn der Ausgang vom Tristate-Zustand auf L wechselt.

t_{PHZ} Sperr-Verzögerungszeit, bis der Ausgang vom H-Pegel in den Tristate-Zustand geht.

t_{PLZ} Sperr-Verzögerungszeit, bis der Ausgang vom L-Pegel in den Tristate-Zustand geht.

t_W Eingangssignal-Impulsbreite.

t_S Eingangs-Vorbereitungszeit. Es ist die Zeit, um die die Daten eher anliegen müssen, als der Taktimpuls kommt.

t_H Eingangs-Haltezeit. Es ist die Zeit, während der die Daten noch anliegen müssen, nachdem der Taktimpuls gekommen ist.

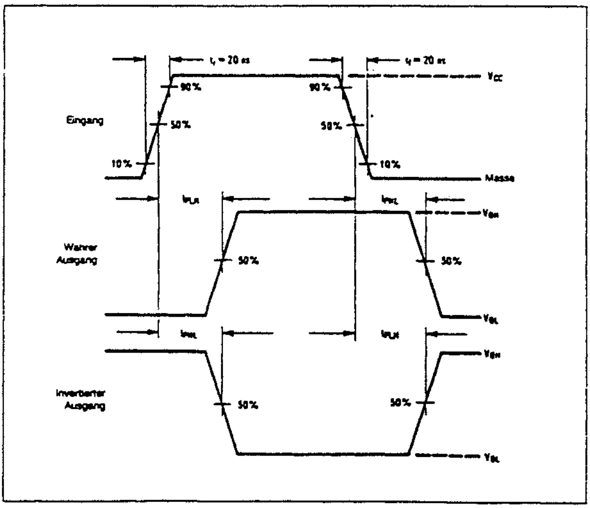
t_{REM} Vorbereitungszeit für den Takt. Es ist die Zeit, die zwischen Wegnahme von irgendwelchen Lösch- oder Freigabesignalen und dem Eintreffen des Taktimpulses mindestens erforderlich ist. Sie wird manchmal auch als Erholungszeit bezeichnet.

t_r Anstiegszeit des Eingangssignals.

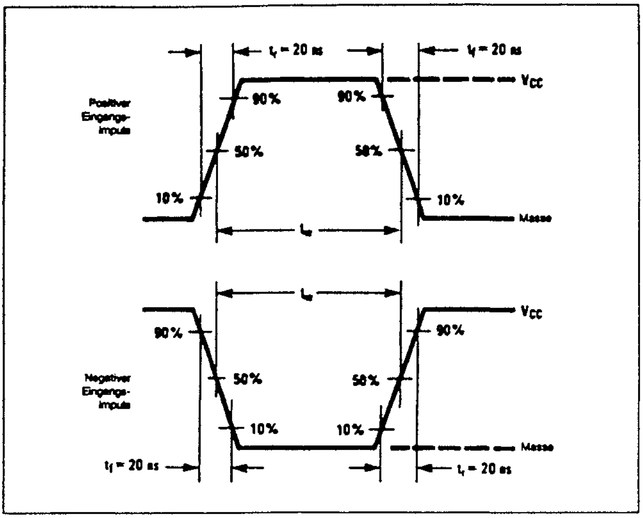
t_f Abfallzeit des Eingangssignals.

t_{TLH} Anstiegszeit des Ausgangs (Übergang von L nach H).

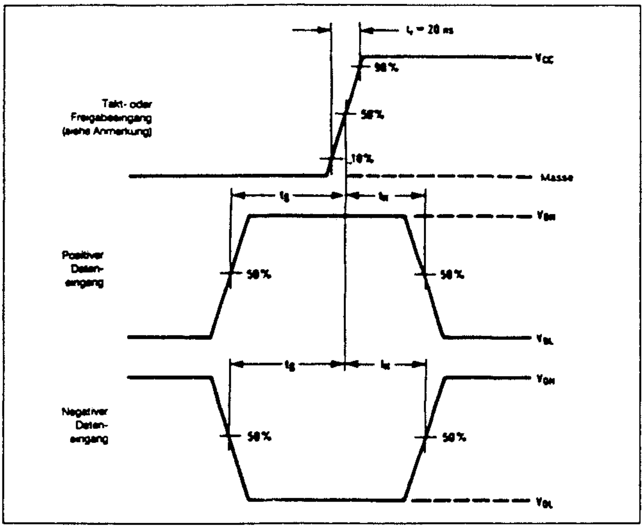
t_{THL} Abfallzeit des Ausgangs (Übergang von H nach L).



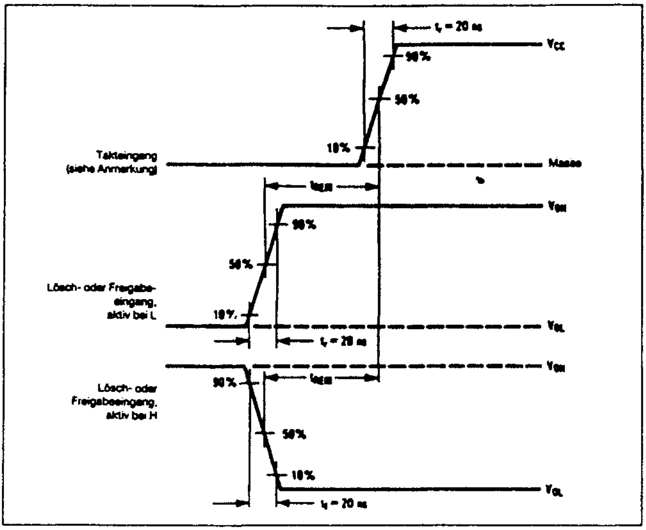
Übertragungsverzögerung



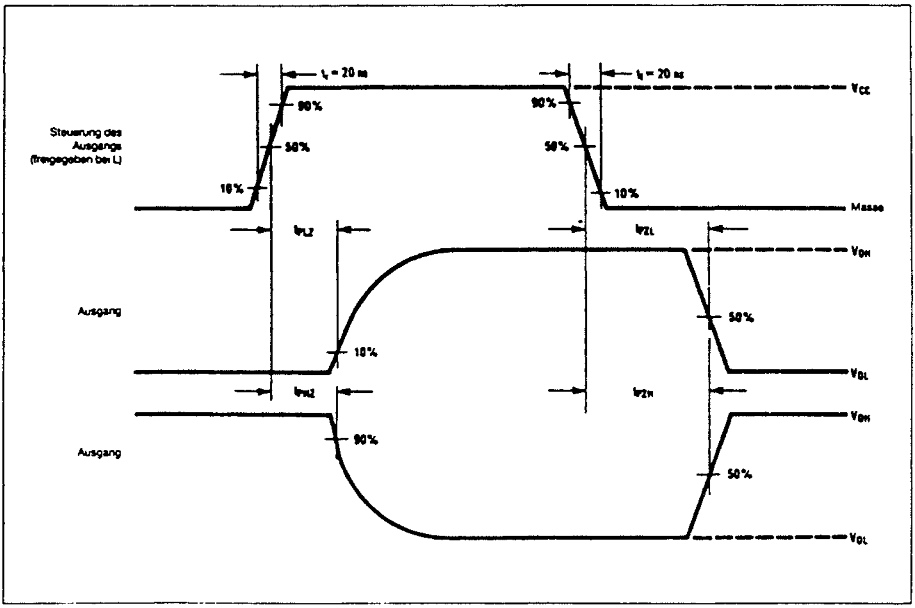
Kurvenform des Eingangsimpulses



Kurvenläufe der Vorbereitungs- und Haltezeit



Kurvenverlauf der Erholungszeit



Kurvenformen bei Freigabe und Sperren des Tristate-Ausgangs

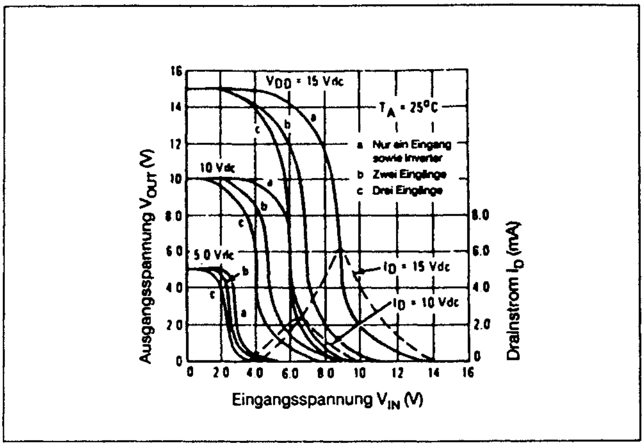
Zwei NOR-Gatter mit je 3 Eingängen plus Inverter

Allgemeine Betriebskenngrößen

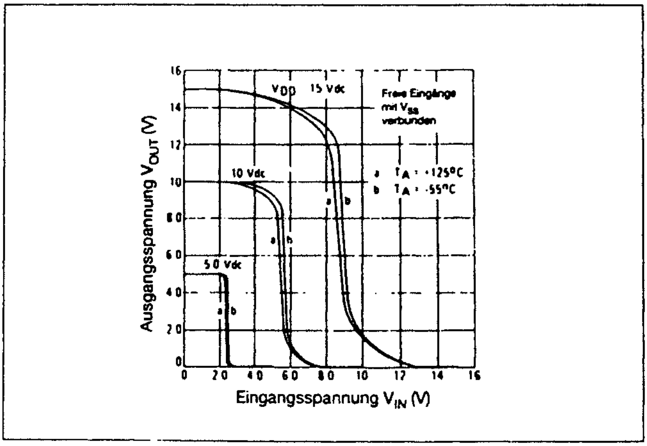
Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0	—	0	0,05	V
		10	—	0	0,05	
		15	—	0	0,05	
Ausgangsspannung V_{OH}		5,0	4,95	5,0	—	V
		10	9,95	10	—	
		15	14,95	15	—	
Eingangsspannung V_{IL}		5,0	—	2,25	1,0	V
		10	—	4,50	2,0	
		15	—	6,75	2,5	
Eingangsspannung V_{IH}		5,0	4,0	2,75	—	V
		10	8,0	5,50	—	
		15	12,5	8,25	—	
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V	5,0	—0,8	—1,7	—	mA
	V_{OH} = 4,6 V	5,0	—0,16	—0,36	—	
	V_{OH} = 9,5 V	10	—0,4	—0,9	—	
	V_{OH} = 13,5 V	15	—1,2	—3,5	—	
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V	5,0	0,44	0,88	—	mA
	V_{OL} = 0,5 V	10	1,1	2,25	—	
	V_{OL} = 1,5 V	15	3,0	8,8	—	
Ruhestrom I_{DD}		5,0	—	0,0005	1,0	µA
		10	—	0,0010	2,0	
		15	—	0,0015	4,0	



Typische Strom- und Spannungsübertragung



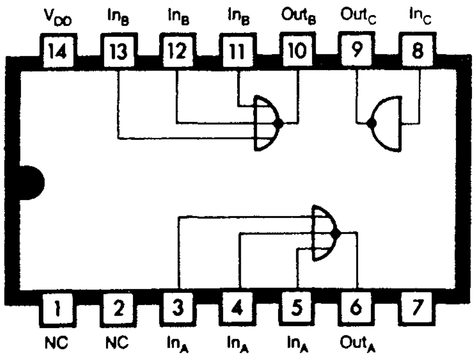
Typische Spannungsübertragung

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	µA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	180 90 65	360 180 130	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	115 55 40	230 110 80	ns

Anschlußbelegung



4001 Vier NOR-Gatter mit je 2 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

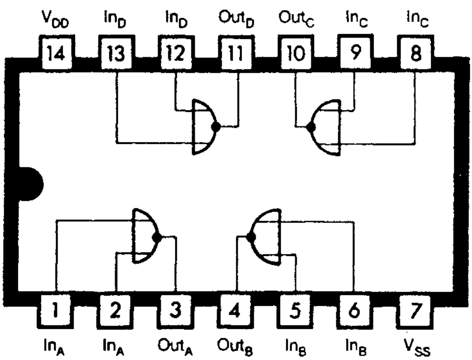
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— — —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

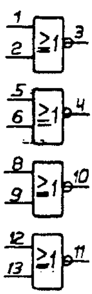
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	250 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	125 50 40	250 100 80	ns

Anschlußbelegung





4002 Zwei NOR-Gatter mit je 4 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

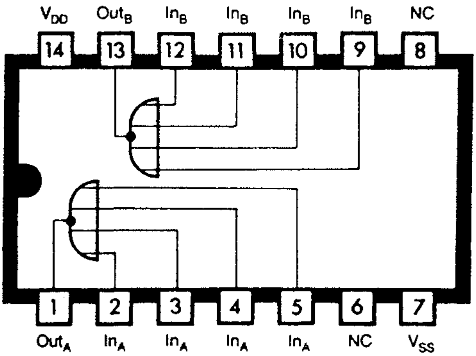
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— — —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

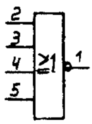
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

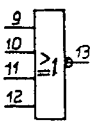
Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	160 65 50	300 130 100	ns

Anschlußbelegung







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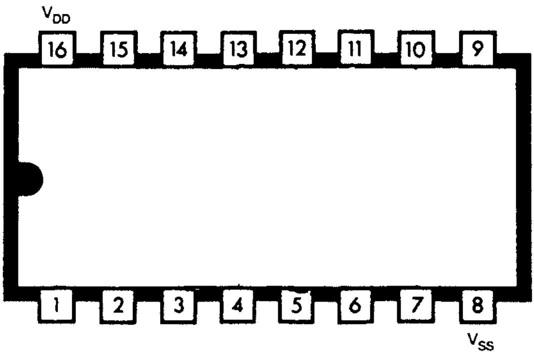
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Ruhestrom I_{DD}	5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	μA
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

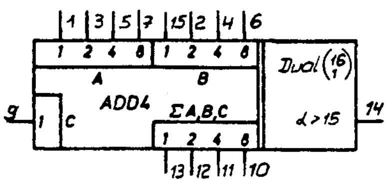
Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	180 90 65	360 180 130	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	115 55 40	200 110 85	ns

Anschlußbelegung



Wahrheitstabelle

C	B_n	A_n	S_n	α>15
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



4011 Vier NAND-Gatter mit je 2 Eingängen

4012 Zwei NAND-Gatter mit je 4 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

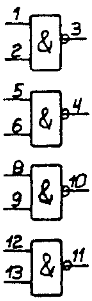
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0	—	0	0,05	V
		10	—	0	0,05	
		15	—	0	0,05	
Ausgangsspannung V_{OH}		5,0	4,95	5,0	—	V
		10	9,95	10	—	
		15	14,95	15	—	
Eingangsspannung V_{IL}		5,0	—	2,25	1,0	V
		10	—	4,50	3,0	
		15	—	6,75	4,0	
Eingangsspannung V_{IH}		5,0	3,5	2,75	—	V
		10	7,0	5,50	—	
		15	11,0	8,25	—	
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V	5,0	—2,1	—4,2	—	mA
	V_{OH} = 4,6 V	5,0	—0,44	—0,88	—	
	V_{OH} = 9,5 V	10	—1,1	—2,25	—	
	V_{OH} = 13,5 V	15	—3,0	—8,8	—	
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V	5,0	0,44	0,88	—	mA
	V_{OL} = 0,5 V	10	1,1	2,25	—	
	V_{OL} = 1,5 V	15	3,0	8,8		
Ruhestrom I_{DD}		5,0	—	0,0005	1,0	µA
		10	—	0,0010	2,0	
		15	—	0,0015	4,0	

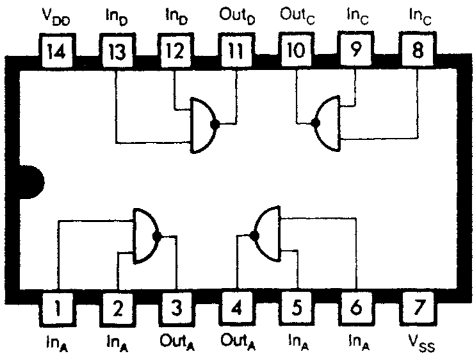
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	125 50 40	250 100 80	ns

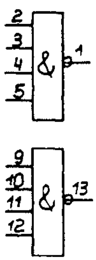
Anschlußbelegung

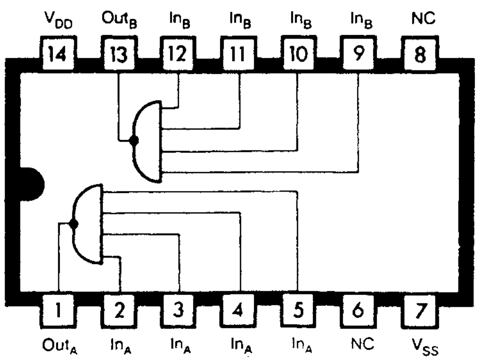




4011

Anschlußbelegung





4012

4013 Zwei D-Flipflops

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	$-0,5$ bis $+18$	V
Eingangsspannung V_{IN}	$-0,5$ bis $V_{DD} + 0,5$	V
Leckstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	-40 bis $+85$	°C
Lagerungstemperatur T_{stg}	-65 bis $+150$	°C

Elektrische Eigenschaften bei $T_A = 25\,°C$

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0	–	0	0,05	V
		10	–	0	0,05	
		15	–	0	0,05	
Ausgangsspannung V_{OH}		5,0	4,95	5,0	–	V
		10	9,95	10	–	
		15	14,95	15	–	
Eingangsspannung V_{IL}		5,0	–	2,25	1,5	V
		10	–	4,50	3,0	
		15	–	6,75	4,0	
Eingangsspannung V_{IH}		5,0	3,5	2,75	–	V
		10	7,0	5,50	–	
		15	11,0	8,25	–	
Ausgangsstrom I_{OH}	$V_{OH} = 2,5$ V	5,0	−2,1	−4,2	–	mA
	$V_{OH} = 4,6$ V	5,0	−0,44	−0,88	–	
	$V_{OH} = 9,5$ V	10	−1,1	−2,25	–	
	$V_{OH} = 13,5$ V	15	−3,0	−8,8	–	
Ausgangsstrom I_{OL}	$V_{OL} = 0,4$ V	5,0	0,44	0,88	–	mA
	$V_{OL} = 0,5$ V	10	1,1	2,25	–	
	$V_{OL} = 1,5$ V	15	3,0	8,8	–	
Ruhestrom I_{DD}		5,0	–	0,002	4,0	µA
		10	–	0,004	8,0	
		15	–	0,006	16	

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	–	± 0,00001	± 0,3	μA
Eingangskapazität C_{IN}	–	–	5,0	7,5	pF
Tristate Reststrom I_{TL}	15	–	–	–	μA

Schaltverhalten bei C_L = 50 pF und T_A = 25 °C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Ausgangsabfallszeit t_{THL}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Taktfrequenz f_{cl}	5,0 10 15	– – –	2,0 5,0 7,0	4,0 10 14	MHz
Taktimpulsbreite t_{WL}, t_{WH}	5,0 10 15	125 50 35	250 100 70	– – –	ns
Taktimpulsanstiegs- und Abfallszeit t_{THL}, t_{TLH}	5,0 10 15	– – –	– – –	15 5,0 4,0	μs
Vorbereitungszeit t_{su}	5,0 10 15	– – –	20 10 7,5	40 20 15	ns
Haltezeit t_h	5,0 10 15	20 10 7,5	40 20 15	– – –	ns
Setimpulsbreite t_{WL}	5,0 10 15	125 50 35	250 100 70	– – –	ns
Resetimpulsbreite t_{WH}	5,0 10 15	125 50 35	250 100 70	– – –	ns

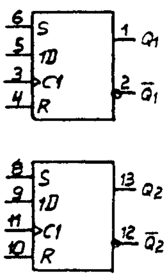
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Verzögerungszeit t_{PLH}, t_{PHL} auf Q takten	5,0 10 15	– – –	175 75 50	350 150 100	ns
Verzögerungszeit t_{PHL}, t_{PHL} auf Q setzen	5,0 10 15	– – –	175 75 50	350 150 100	ns
Verzögerungszeit t_{PHL}, t_{PHL}, auf Q zurücksetzen	5,0 10 15	– – –	350 100 75	450 200 150	

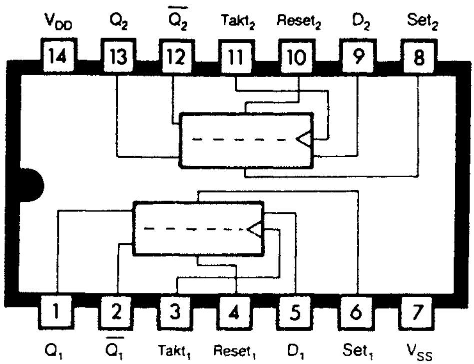
Wahrheitstabelle

Eingänge				Ausgänge	
Takt	Daten	Reset	Set	Q	$\overline{Q}$
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	NC	
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = irrelevant
NC = kein Wechsel

Anschlußbelegung



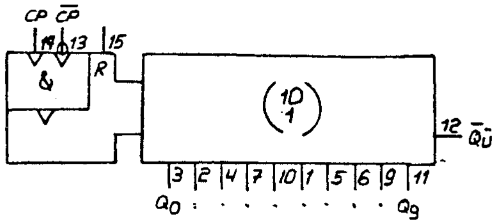


Johnson-Dezimalzähler-Teiler

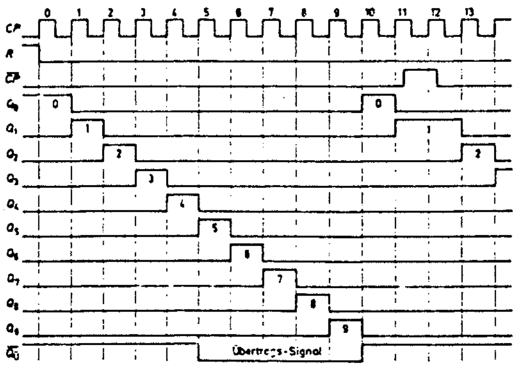
Der Johnson-Dezimalzähler-Teiler enthält 10 dezimal codierte Ausgänge und einen Übertragsausgang. Der Zähler-Teiler ist selbststartend und kann mit 0-1-Flanken sowie 1-0-Flanken angesteuert werden.
Dabei kann der jeweils unbenutzte Eingang zum sperrren des Zähl-/Teil-Vorgangs eingesetzt werden.

Wahrheitstabelle

CP	$\overline{CP}$	R	Q_0	Q_1 bis Q_9	$\overline{Q_Ü}$
X	X	1	1	0	1
↑	0	0	Zähler weitergestellt		
1	↓	0	Zähler weitergestellt		
X	1	0	keine Änderung		
0	X	0	keine Änderung		
↓	0	0	keine Änderung		
1	↑	0	keine Änderung		



Zeitdiagramm



Kurzdaten

Speisespannung	U_{DD}	=	3...15 V
Max. Umgebungstemperaturbereich	ϑ_U	=	-40...+85 °C
Typ. Zählfrequenz bei U_{DD} = 10 V, ϑ_U = 25 °C	f_{CP}	=	0...13,8 MHz
Ausgangsstrom bei $U_{Q\,L}$ = 0,4 V, U_{DD} = 5 V	$I_{Q\,L}$	=	0,4 mA
Ruhestrom pro Gehäuse bei U_{DD} = 5 V, ϑ_U = 25 °C	I_{DDmax}	=	50 µA

4019 Vierfach 2-Kanal-Multiplexer/Demultiplexer

Elektrische Eigenschaften bei $T_A = 25$ °C

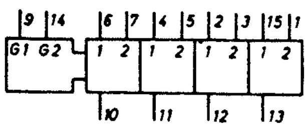
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

Schaltverhalten bei $C_L = 50$ pF und $T_A = 25$°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	160 65 50	300 130 100	ns

Wahrheitstabelle

G1	G2	1	2	Q_n
0	0	X	X	0
0	1	X	0	0
0	1	X	1	1
1	0	0	X	0
1	0	1	X	1
1	1	1	X	1
1	1	X	1	1
1	1	0	0	0



4023 Drei NAND-Gatter mit je 3 Eingängen

4025 Drei NOR-Gatter mit je 3 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

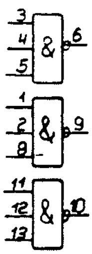
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2.0 4,0	µA

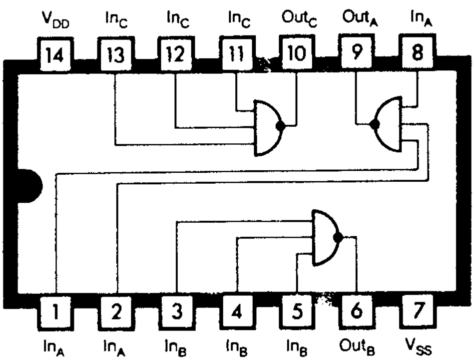
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	160 65 50	300 130 100	ns

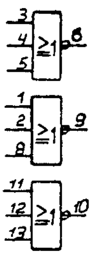
Anschlußbelegung

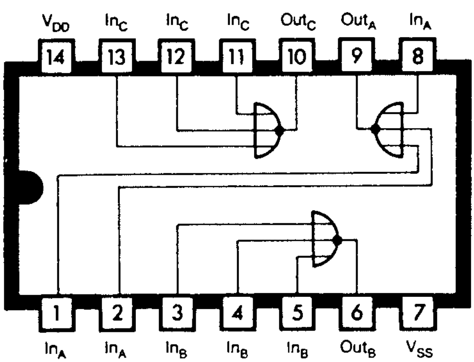




4023

Anschlußbelegung





4025

Zwei J-K-Flipflops

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis + 18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
Leckstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis + 85	°C
Lagerungstemperatur T_{stg}	−65 bis + 150	°C

Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	– – –	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	– – –	V
Eingangsspannung V_{IL}		5,0 10 15	– – –	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	– – –	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	−2,1 −0,44 −1,1 −3,0	−4,2 −0,88 −2,25 −8,8	– – – –	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	– – –	mA
Ruhestrom I_{DD}		5,0 10 15	– – –	0,002 0,004 0,006	4,0 8,0 16	µA

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	–	± 0,00001	± 0,3	µA
Eingangskapazität C_{IN}	–	–	5,0	7,5	pF
Tristate Reststrom I_{TL}	15	–	–	–	µA

Schaltverhalten bei C_L = 50 pF und T_A = 25 °C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Ausgangsabfallszeit t_{THL}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Taktfrequenz f_{cl}	5,0 10 15	– – –	1,5 4,5 6,5	3,0 9,0 13	MHz
Taktimpulsbreite t_{WL}, t_{WH}	5,0 10 15	165 55 38	330 110 75	– – –	ns
Taktimpulsanstiegs- und Abfallszeit t_{THL}, t_{TLH}	5,0 10 15	– – –	– – –	15 5,0 4,0	µs
Vorbereitungszeit t_{su}	5,0 10 15	– – –	70 25 17	140 50 35	ns
Haltezeit t_h	5,0 10 15	70 25 17	140 50 35	– – –	ns
Setimpulsbreite t_{WL}	5,0 10 15	125 50 35	250 100 70	– – –	ns
Resetimpulsbreite t_{WH}	5,0 10 15	125 50 35	250 100 70	– – –	ns

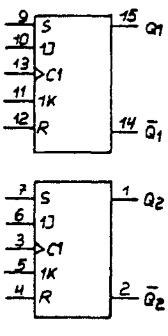
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Verzögerungszeit t_{PLH}, t_{PHL} auf Q takten	5,0 10 15	– – –	175 75 50	350 150 100	ns
Verzögerungszeit t_{PHL}, t_{PHL} auf Q setzen	5,0 10 15	– – –	175 75 50	350 150 100	ns
Verzögerungszeit t_{PHL}, t_{PHL}, auf Q zurücksetzen	5,0 10 15	– – –	350 100 75	450 200 150	

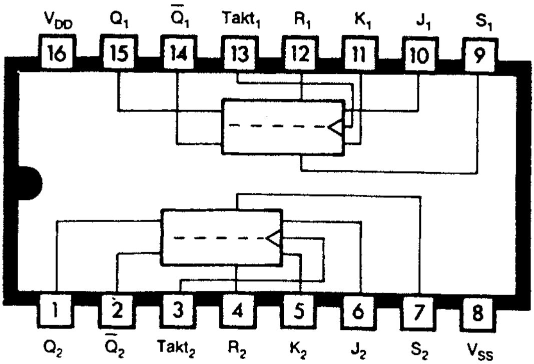
Wahrheitstabelle

Eingänge					Ausgänge		
Takt	J	K	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↑	1	1	0	0	Q_0	$\overline{Q_0}$	Q_0
↓	X	X	0	0	X	NC	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = irrelevant
NC = kein Wechsel

Anschlußbelegung





Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis +30	V
max. Strom I (je Eingangsanschluß)	10	mA
max. Strom I (je Ausgangsanschluß)	45	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

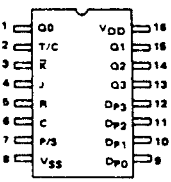
Allgemeine Hinweise

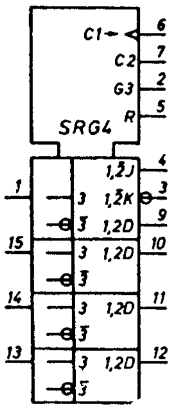
Die CMOS-Schaltung 4035 enthält ein einflankengesteuertes 4 bit Schieberegister, das über den Eingang C2 (parallel enable) von Parallel- (C2 = HIGH) auf Serienbetrieb (C2 = LOW) umschaltbar ist. Die Informationsübernahme erfolgt sowohl im Parallelbetrieb (Eingänge 1D) als auch im Serienbetrieb (Eingänge J, K) mit der 0/1-Flanke des Taktsignals an C1. Die Schaltung ist mit einem gemeinsamen G3-Eingang (true/complement) und einem gemeinsamen Rückstelleingang R versehen.

Wahrheitstabellen

C1	1J	1K	C2	1D	Q_n^{n+1}
↑	0	0	0	X	0
↑	0	1	0	X	keine Änderungen
↑	1	0	0	X	$\overline{Q}_n$
↑	1	1	0	X	1
↑	X	X	1	1	1D
↑	X	X	1	0	$\overline{1D}$
↓	X	X	X	X	keine Änderungen

R	G3	Q_n
1	1	0
1	0	1
0	1	Q_n
0	0	$\overline{Q}_n$





Allgemeine Betriebskenngrößen

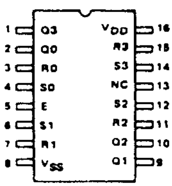
Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis +18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis +85	°C
Lagerungstemperatur T_{stg}	−65 bis +150	°C

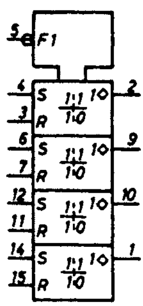
Schaltverhalten bei C_L = 50 pF und T_A = 25 °C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Ausgangsabfallszeit t_{THL}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Taktfrequenz f_{cl}	5,0 10 15	– – –	1,8 4,5 6,0	3,6 9,0 12	MHz
Taktimpulsbreite t_{WL}, t_{WH}	5,0 10 15	130 55 40	260 110 80	– – –	ns
Taktimpulsanstiegs- und Abfallszeit t_{THL}, t_{TLH}	5,0 10 15	– – –	– – –	1,5 5 4	µs
Vorbereitungszeit t_{su}	5,0 10 15	– – –	110 40 25	220 40 25	ns

Wahrheitstabelle

F1	S_n	R_n	Q_n
0	X	X	Ausgänge abgetrennt
1	1	0	1
1	0	1	0
1	1	1	1
1	0	0	keine Änderung





Erweiterbares Gatter mit 8 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis +18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis +85	°C
Lagerungstemperatur T_{stg}	−65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	– – –	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5 10 15	– – –	V
Eingangsspannung V_{IL}		5,0 10 15	– – –	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	– – –	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	−1,36 −0,44 −1,1 −3,0	−3,2 −1 −2,6 −6,8	– – – –	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	1 2,6 6,8	– – –	mA
Ruhestrom I_{DD}		5,0 10 15	– – –	0,01 0,01 0,01	1 2 4	μA

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	–	± 0,00001	± 0,3	μA
Eingangskapazität C_{IN}	–	–	5,0	7,5	pF
Tristate Reststrom I_{TL}	15	–	± 0,0001	± 1,0	μA

Schaltverhalten bei $C_L = 50$ pF und $T_A = 25$ °C

Ausgangsanstiegszeit t_{TLH}	5,0	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Ausgangsabfallszeit t_{THL}	5,0	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Verzögerungszeit t_{PLH}, t_{PHL} (Steuereingang k_a)	5,0	–	300	600	ns
	10	–	150	300	
	15	–	120	240	
Verzögerungszeit t_{PHL}, t_{PLH} (Steuereingang k_b)	5,0	–	225	450	ns
	10	–	85	170	
	15	–	55	110	
Verzögerungszeit t_{PLH}, t_{PHL} (Steuereingang k_c)	5,0	–	140	280	ns
	10	–	50	100	
	15	–	40	80	
Verzögerungszeit t_{PLH}, t_{PHL} (Erweiterungseingang)	5,0	–	190	380	ns
	10	–	90	180	
	15	–	65	130	
Tristate Verzögerung t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PHZ} (Steuereingang k_d)	5,0	–	80	160	ns
	10	–	35	70	
	15	–	25	50	

Betrieb des Mehrfunktionsgatters 4048

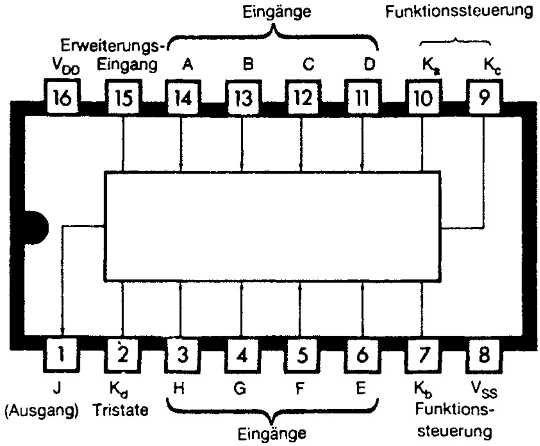
Je nach Ansteuerung der drei binären Steuerleitungen k_a, k_b und k_c können 8 verschiedene Logikfunktionen eingestellt werden, und zwar ODER, NOR, UND, NAND, ODER/UND, ODER/NAND, UND/ODER und UND/NOR (siehe Wahrheitstabelle). Ein vierter Eingang k_d ermöglicht eine Tristate-Steuerung des Ausganges, wodurch ein Anschluß an eine gemeinsame Busleitung möglich ist. Wenn k_d high ist, wird der Ausgang freigegeben. Ist k_d low, besitzt der Ausgang eine hohe Impedanz.

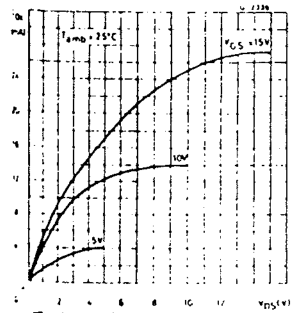
Der Erweiterungseingang (Pin 15) ermöglicht dem Anwender, die Anzahl der Gattereingänge zu vergrößern. Beispielsweise können zwei 4048 zu einem Mehrfunktionsgatter mit 16 Eingängen kaskadiert werden. Wenn der Erweiterungseingang nicht verwendet wird, sollte er an Masse gelegt werden.

Wahrheitstabelle

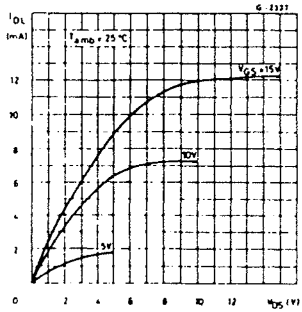
Ausgangsfunktion	Boole'sche Gleichung	Steuereingänge k_a	k_b	k_c	k_d	Anschluß der nichtbenutzten Eingänge an
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	1	V_{SS}
ODER	$J = A+B+C+D+E+F+G+H$	0	0	1	1	V_{SS}
ODER/UND	$J = (A+B+C+D) \cdot (E+F+G+H)$	0	1	0	1	V_{SS}
ODER/NAND	$J = \overline{(A+B+C+D) \cdot (E+F+G+H)}$	0	1	1	1	V_{SS}
UND	$J = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$	1	0	1	1	V_{DD}
UND/NOR	$J = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$	1	1	0	1	V_{DD}
UND/ODER	$J = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$	1	1	1	1	V_{DD}
hochohmig		X	X	X	0	X = irrelevant

Anschlußbelegung

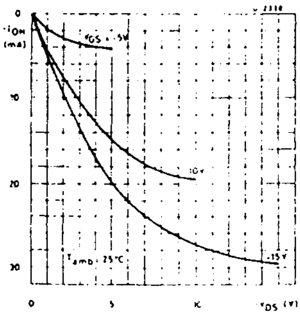




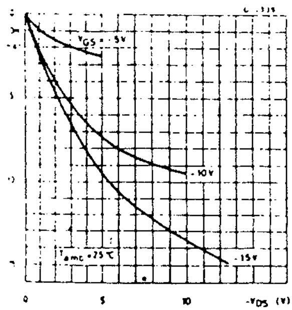
Typischer Ausgangssenkenstrom
(Ausgang: low)



Minimaler Ausgangssenkenstrom
(Ausgang: low)



Typischer Ausgangsquellenstrom
(Ausgang: high)



Minimaler Ausgangsquellenstrom
(Ausgang: high)

4049 Sechs invertierende Puffer

4050 Sechs nichtinvertierende Puffer

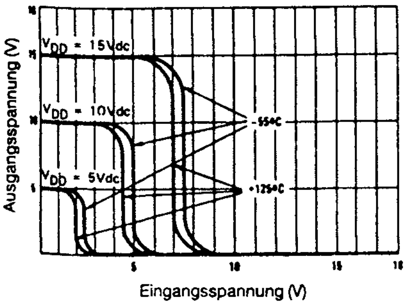
Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis +0,30	V
max. Strom I (je Eingangsanschluß)	10	mA
max. Strom I (je Ausgangsanschluß)	45	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

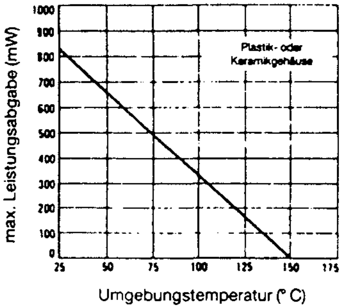
Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,0 2,0 2,5	V
Eingangsspannung V_{IH}		5,0 10 15	4,0 8,0 12,5	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—1,25 — —1,3 —3,75	—2,5 — —2,6 —10	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,2 8,0 24	6,0 16 40	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,002 0,004 0,006	4,0 8,0 16	μA

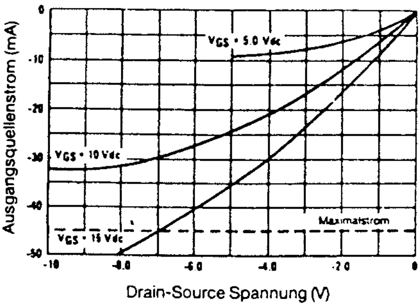
Spannungsübertragungs-Kennlinie



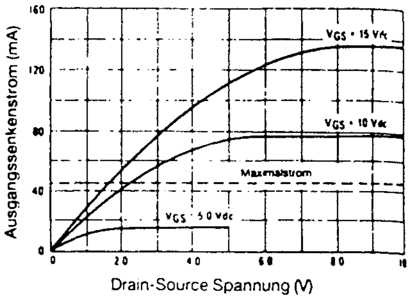
Leistungsabgabe



Ausgangsquellen-Kennlinie



Ausgangssenken-Kennlinie

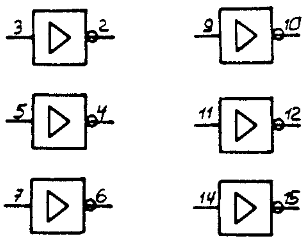


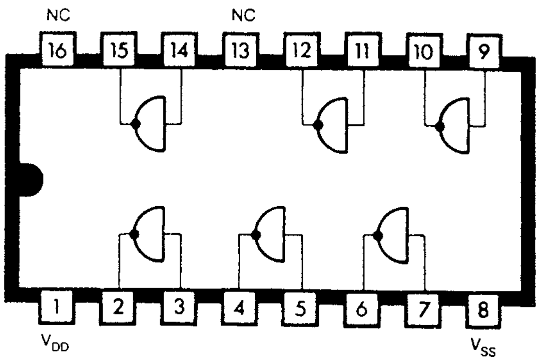
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	µA
Eingangskapazität C_{IN}	—	—	10	20	pF
Tristate Reststrom I_{TL}	15	—	—	—	µA

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

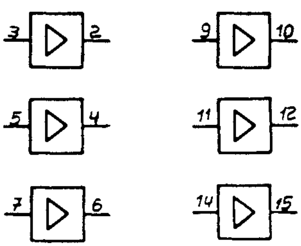
Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	160 80 60	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	40 20 15	60 40 30	ns
Verzögerungszeit t_{PLH}	5,0 10 15	— — —	80 40 30	140 80 60	ns
Verzögerungszeit t_{PHL}	5,0 10 15	— — —	40 20 15	80 40 30	ns

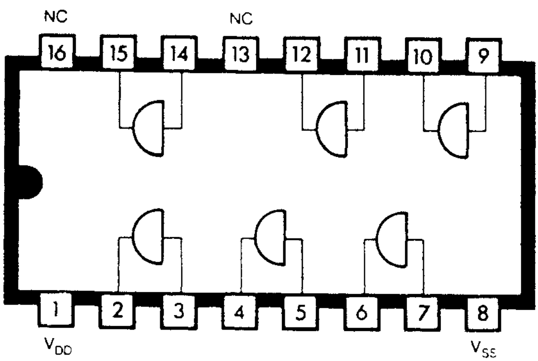
Anschlußbelegung 4049





Anschlußbelegung 4050





Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis + 18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis + 85	°C
Lagerungstemperatur T_{stg}	−65 bis + 150	°C

Allgemeine Hinweise

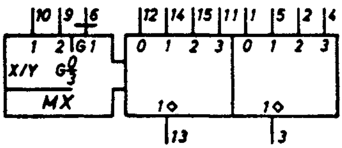
Die CMOS-Schaltung 4052 enthält zwei mal vier stromrichtungsunabhängige Schalter (transmission gates), von denen jeweils zwei durch eine 2 bit Adresse dekodiert, d.h. in den niederohmigen "EIN"-Zustand geschaltet werden. Das Sperren aller Schalter erfolgt mit HIGH am Inhibit-Eingang

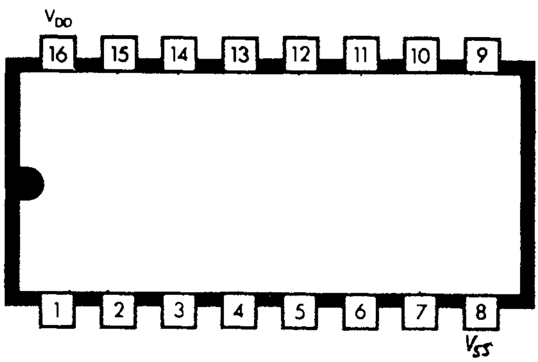
Zum Schalten anderer Spannungen als der Logikspannung U_{DD}-U_{SS} ist ein Speisespannungsanschluß U_{EE} herausgeführt, der mit dem niedrigsten Potential der zu schaltenden Spannung verbunden sein muß. Die Spannung U_{DD} gegen U_{EE} darf 15 V nicht überschreiten. Normalerweise ist U_{EE} mit U_{SS} verbunden; U_{EE} darf jedoch negativ gegen U_{SS} werden.

Wahrheitstabelle

G1	2	1	"EIN"-Zustand für
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	keiner (alle Schalter hochohmig)

Anschlußbelegung





4069 Sechs Inverter

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

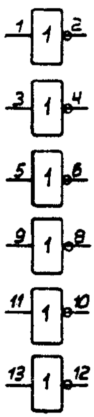
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,0 2,0 2,5	V
Eingangsspannung V_{IH}		5,0 10 15	4,0 8,0 12,5	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

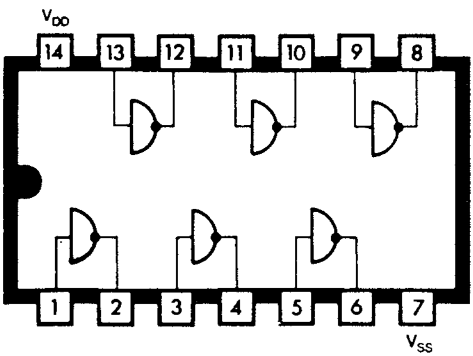
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	65 40 30	125 75 55	ns

Anschlußbelegung





4070 Vier Exklusiv-OR-Gatter mit je 2 Eingängen

4077 Vier Exklusiv-NOR-Gatter mit je 2 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

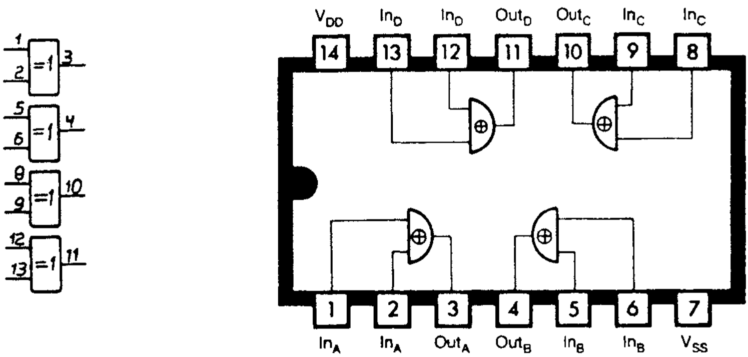
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

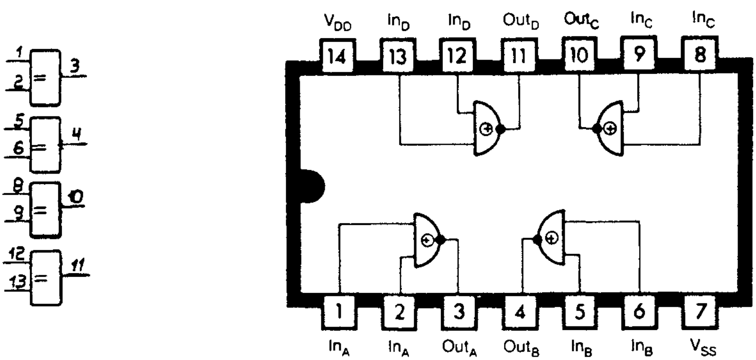
Schaltverhalten bei C_L = 50 pF und T_A = 25°C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	175 75 50	350 150 100	ns

Anschlußbelegung 4070



Anschlußbelegung 4077



4071 Vier OR-Gatter mit je 2 Eingängen

4072 Zwei OR-Gatter mit je 4 Eingängen

4073 Drei AND-Gatter mit je 3 Eingängen

4075 Drei OR-Gatter mit je 3 Eingängen

4081 Vier AND-Gatter mit je 2 Eingängen

4082 Zwei AND-Gatter mit je 4 Eingängen

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	—0,5 bis +18	V
Eingangsspannung V_{IN}	—0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	—40 bis + 85	°C
Lagerungstemperatur T_{stg}	—65 bis +150	°C

Elektrische Eigenschaften bei T_A = 25 °C

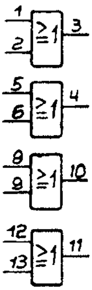
Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	— — —	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	— — —	V
Eingangsspannung V_{IL}		5,0 10 15	— — —	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	— — —	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	—2,1 —0,44 —1,1 —3,0	—4,2 —0,88 —2,25 —8,8	— — — —	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	— —	mA
Ruhestrom I_{DD}		5,0 10 15	— — —	0,0005 0,0010 0,0015	1,0 2,0 4,0	µA

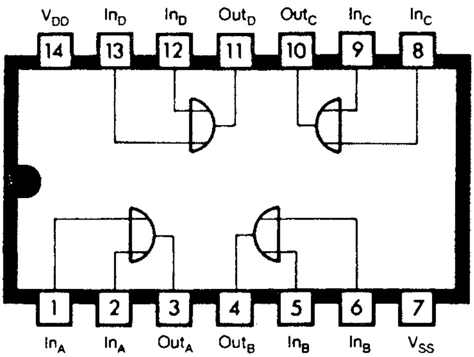
Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	—	±0,00001	±0,3	μA
Eingangskapazität C_{IN}	—	—	5,0	7,5	pF

Schaltverhalten bei C_L = 50 pF und T_A = 25°C

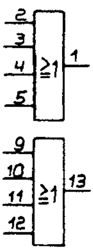
Ausgangsanstiegszeit t_{TLH}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Ausgangsabfallzeit t_{THL}	5,0 10 15	— — —	100 50 40	200 100 80	ns
Verzögerungszeit t_{PLH}, t_{PHL}	5,0 10 15	— — —	160 65 50	300 130 100	ns

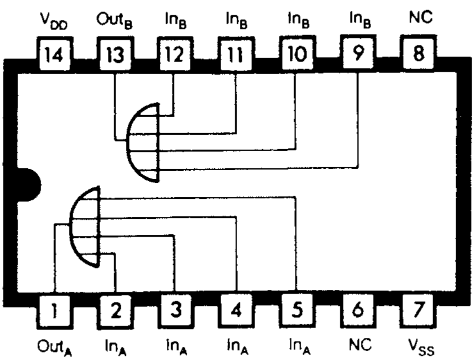
Anschlußbelegung 4071

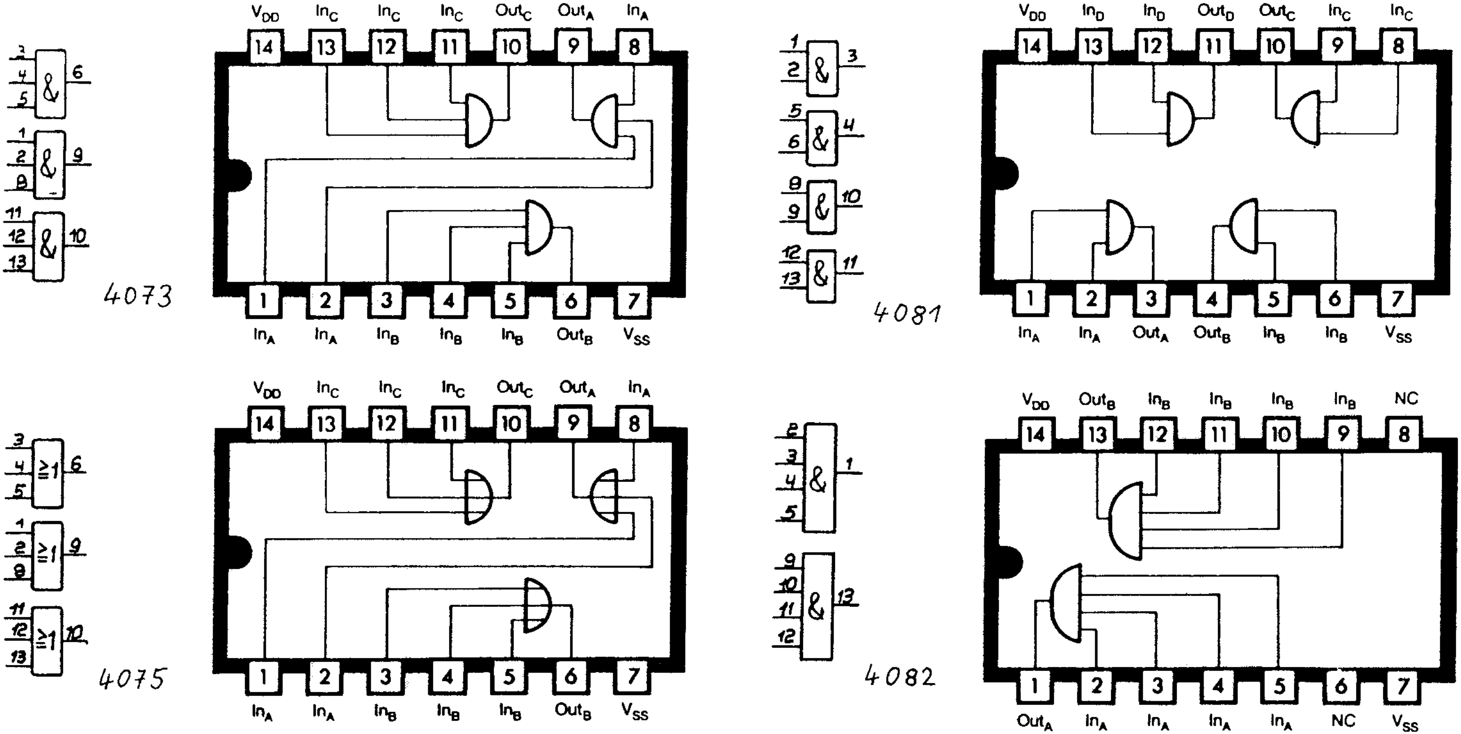




Anschlußbelegung 4072







Anschlußbelegung

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O 4.5 or 0.5 Vdc)		5.0	–	1.5	–	–	1.5	–	1.5	
(V_O 9.0 or 1.0 Vdc)		10	–	3.0	–	–	3.0	–	3.0	
(V_O 13.5 or 1.5 Vdc)		15	–	4.0	–	–	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O · 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	–	–	3.5	–	Vdc
(V_O · 1.0 or 9.0 Vdc)		10	7.0	–	7.0	–	–	7.0	–	
(V_O · 1.5 or 13.5 Vdc)		15	11.0	–	11.0	–	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4 µA/kHz) f + I_{DD}							
		15	I_T = (3.6 µA/kHz) f + I_{DD}							
Hysteresis Voltage (Pins 2, 5, 9, 12, held high)	V_H#	5.0	0.20	0.42	0.17	0.28	0.39	0.13	0.39	Vdc
		10	0.29	0.66	0.25	0.38	0.60	0.20	0.60	
		15	0.39	1.00	0.33	0.50	0.90	0.27	0.90	
Threshold Voltage (Pins 2, 5, 9, 12, held high) Positive-Going	V_{T+}	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
		10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	
		15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	
Negative-Going	V_{T-}	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.06	6.08	2.60	6.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

Output Fall Time	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0 10 15	– – –	125 50 40	250 100 80	ns

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

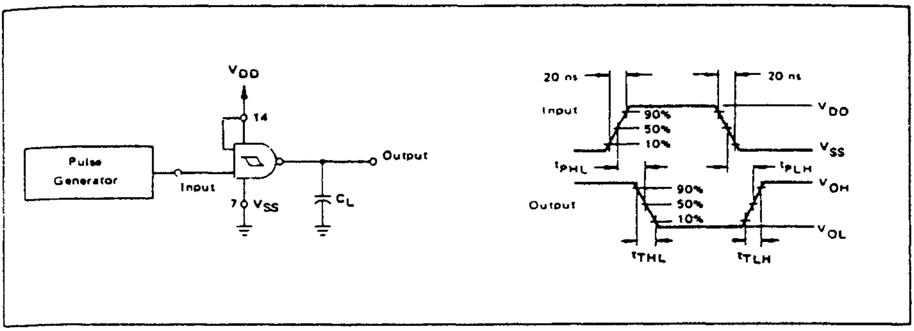
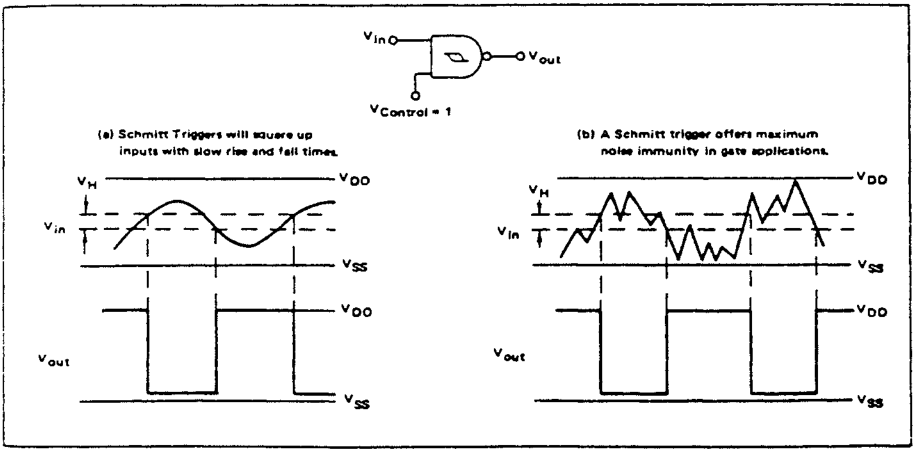
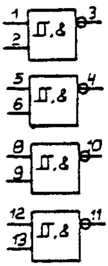


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



Anschlußbelegung



40174 Sechsfach-D-Flipflop

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis + 18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis + 85	°C
Lagerungstemperatur T_{stg}	−65 bis + 150	°C

Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	– – –	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 5,95 14,95	5 10 15	– – –	V
Eingangsspannung V_{IL}		5,0 10 15	– – –	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	– – –	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	−1,36 −0,44 −1,1 −3,0	−3,2 −1,0 −2,6 −6,8	– – – –	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	1,0 2,6 6,8	– – –	mA
Ruhestrom I_{DD}		5,0 10 15	– – –	0,02 0,02 0,02	4 8 16	µA

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	–	± 0,00001	± 0,3	µA
Eingangskapazität C_{IN}	–	–	5,0	7,5	pF
Tristate Reststrom I_{TL}	15	–	–	–	µA

Schaltverhalten bei C_L = 50 pF und T_A = 25 °C

Ausgangsanstiegszeit t_{TLH}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Ausgangsabfallszeit t_{THL}	5,0 10 15	– – –	100 50 40	200 100 80	ns
Taktfrequenz f_{cl}	5,0 10 15	– – –	3,5 6 8	7 12 16	MHz
Taktimpulsbreite t_{WL}, t_{WH}	5,0 10 15	65 30 20	130 60 40	– – –	ns
Taktimpulsanstiegs- und Abfallszeit t_{THL}, t_{TLH}	5,0 10 15	– – –	– – –	15 15 15	µs
Vorbereitungszeit t_{su}	5,0 10 15	– – –	20 10 0	40 20 10	ns
Haltezeit t_h	5,0 10 15	40 20 15	80 40 30	– – –	ns
Eingangsimpulsbreite für $\overline{\text{CLEAR}}$ t_{WL}	5,0 10 15	50 25 20	100 50 40	– – –	ns
$\overline{\text{CLEAR}}$ Erholungszeit t_{rem}	5,0 10 15	– – –	0 0 0	40 15 10	ns
Verzögerungszeit t_{PLH}, t_{PHL} (Takt zu Ausgang)	5,0 10 15	– – –	150 70 50	300 140 100	ns
Verzögerungszeit t_{PHL} $\overline{\text{CLEAR}}$ zu Ausgang	5,0 10 15	– – –	100 50 40	200 100 80	ns

Wahrheitstabelle

Eingänge			Ausgang
Takt	D	$\overline{\text{CLEAR}}$	Q
↑	0	1	0
↑	1	1	1
↓	X	1	NC
X	X	0	0

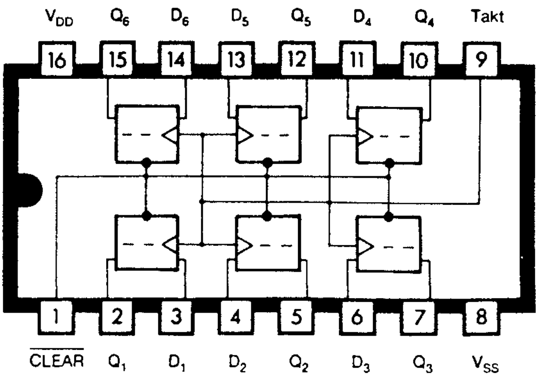
X = irrelevant
NC = kein Wechsel

Funktionsbeschreibung

Dieser Baustein enthält 6 flankengetriggerte D-Flipflops mit sechs Daten-Eingängen und einem gemeinsamen Takt-Eingang sowie einem gemeinsamen Lösch-Eingang.

Die Daten an den D-Eingängen (D_1 bis D_6) werden zu den Ausgängen (Q_1 bis Q_6) bei der positiven Flanke des Taktimpulses an Anschluß 9 übertragen, wenn sich Anschluß 1 ($\overline{\text{CLEAR}}$) auf high befindet. Wird der $\overline{\text{CLEAR}}$-Eingang auf low gebracht, so werden alle Flipflops auf low gesetzt, unabhängig vom Zustand des Takteinganges und der Dateneingänge.

Anschlußbelegung



Vierfach-D-Flipflop

Allgemeine Betriebskenngrößen

Spezifische Daten	Bereich	Einh.
Versorgungsspannung V_{DD}	−0,5 bis + 18	V
Eingangsspannung V_{IN}	−0,5 bis V_{DD} + 0,5	V
max. Eingangsstrom I (je Anschluß)	10	mA
Betriebstemperatur T_A	−40 bis + 85	°C
Lagerungstemperatur T_{stg}	−65 bis + 150	°C

Elektrische Eigenschaften bei T_A = 25 °C

Spezifische Daten		V_{DD}	min.	typ.	max.	Einh.
Ausgangsspannung V_{OL}		5,0 10 15	– – –	0 0 0	0,05 0,05 0,05	V
Ausgangsspannung V_{OH}		5,0 10 15	4,95 9,95 14,95	5,0 10 15	– – –	V
Eingangsspannung V_{IL}		5,0 10 15	– – –	2,25 4,50 6,75	1,5 3,0 4,0	V
Eingangsspannung V_{IH}		5,0 10 15	3,5 7,0 11,0	2,75 5,50 8,25	– – –	V
Ausgangsstrom I_{OH}	V_{OH} = 2,5 V V_{OH} = 4,6 V V_{OH} = 9,5 V V_{OH} = 13,5 V	5,0 5,0 10 15	−2,1 −0,44 −1,1 −3,0	−4,2 −0,88 −2,25 −8,8	– – – –	mA
Ausgangsstrom I_{OL}	V_{OL} = 0,4 V V_{OL} = 0,5 V V_{OL} = 1,5 V	5,0 10 15	0,44 1,1 3,0	0,88 2,25 8,8	– – –	mA
Ruhestrom I_{DD}		5,0 10 15	– – –	0,005 0,010 0,015	20 40 80	µA

Spezifische Daten	V_{DD}	min.	typ.	max.	Einh.
Eingangsstrom I_{IN}	15	–	± 0,00001	± 0,3	µA
Eingangskapazität C_{IN}	–	–	5	7,5	pF
Tristate Reststrom I_{TL}	15	–	–	–	µA

Schaltverhalten bei C_L = 50 pF und T_A = 25 °C

Ausgangsanstiegszeit t_{TLH}	5,0	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Ausgangsabfallszeit t_{THL}	5,0	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Taktfrequenz f_{cl}	5,0	–	2,0	7,0	MHz
	10	–	5,0	12,0	
	15	–	6,5	15,5	
Taktimpulsbreite t_{WL}, t_{WH}	5,0	75	150	–	ns
	10	45	90	–	
	15	35	70	–	
Taktimpulsanstiegs- und Abfallszeit t_{THL}, t_{TLH}	5,0	–	–	15	µs
	10	–	–	5	
	15	–	–	4	
Vorbereitungszeit t_{su}	5,0	–	20	40	ns
	10	–	10	20	
	15	–	0	15	
Haltezeit t_h	5,0	40	80	–	ns
	10	20	40	–	
	15	15	30	–	
$\overline{\text{Reset}}$ Erholungszeit t_{rem}	5,0	125	250	–	ns
	10	50	100	–	
	15	40	80	–	
$\overline{\text{Reset}}$impulsbreite t_{WL}	5,0	100	200	–	ns
	10	50	100	–	
	15	40	80	–	

Wahrheitstabelle

Eingänge			Ausgang
Takt	Daten	$\overline{Reset}$	Q
↑	0	1	0
↑	1	1	1
↓	X	1	NC
X	X	0	0

X = irrelevant
NC = kein Wechsel

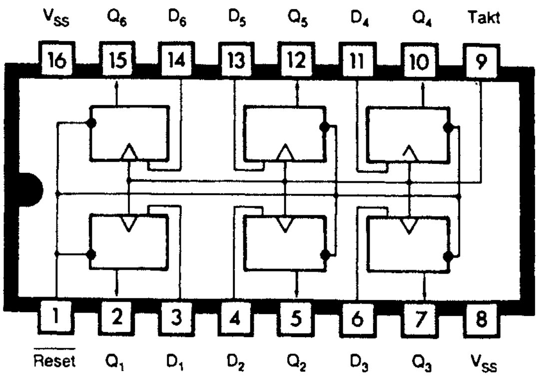
Funktionsbeschreibung

Bei normalem Betrieb muß Anschluß 1 auf high liegen. Zu speichernde Daten werden den D-Eingängen zugeführt. Bei der positiven Flanke des Taktes werden die Informationen an den D-Eingängen intern gespeichert und erscheinen an den entsprechenden Q-Ausgängen.

Wird Anschluß 1 auf Masse gelegt, gehen alle Ausgänge in den low-Zustand.

Dieser Baustein wird zur gleichzeitigen Speicherung von sechs Informationsbits verwendet.

Anschlußbelegung



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}** Min	T_{high}** Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.6 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

TRUTH TABLE

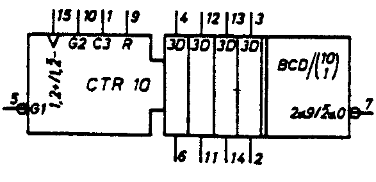
$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

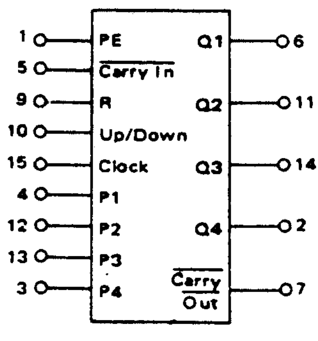
X = Don't Care

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

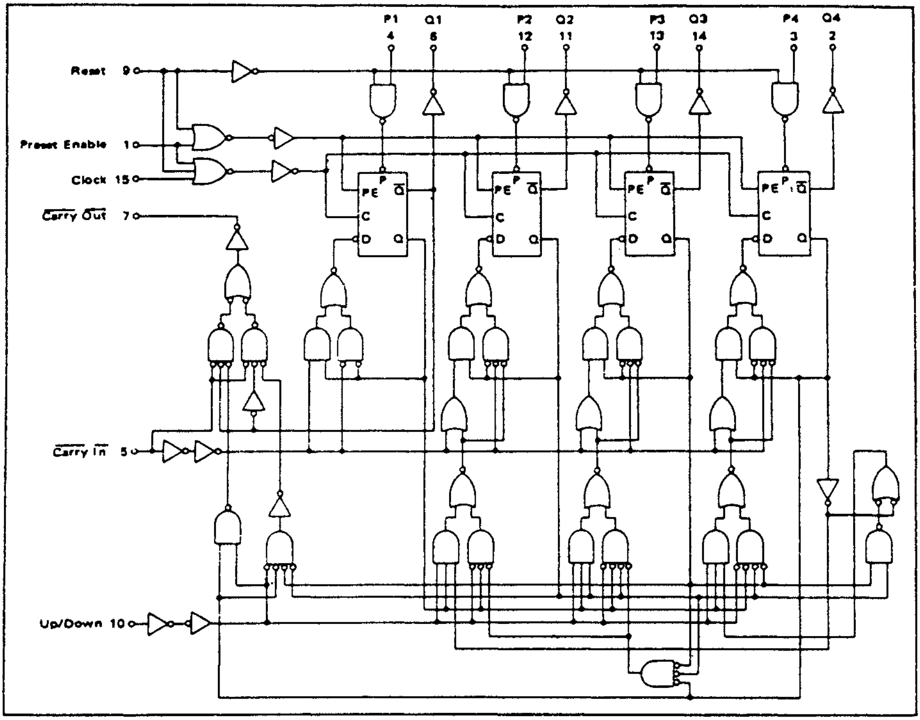
Characteristic	Symbol	V_{DD}	All Types Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L +15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100.	200	
Preset or Reset ot $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Clock Pulse Width	t_{WH}	5.0	350	200	–	ns
		10	170	100	–	
		15	140	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Preset or Reset Removal Time**	t_{rem}	5.0	660	325	–	ns
		10	230	115	–	
		15	180	90	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	15	
		15	–	–	15	
$\overline{\text{Carry In}}$ Setup Time	t_{su}	5.0	200	130	–	ns
		10	120	60	–	
		15	100	50	–	
Up/Down Setup Time	t_{su}	5.0	500	250	–	ns
		10	200	100	–	
		15	175	75	–	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	

Anschlußbelegung

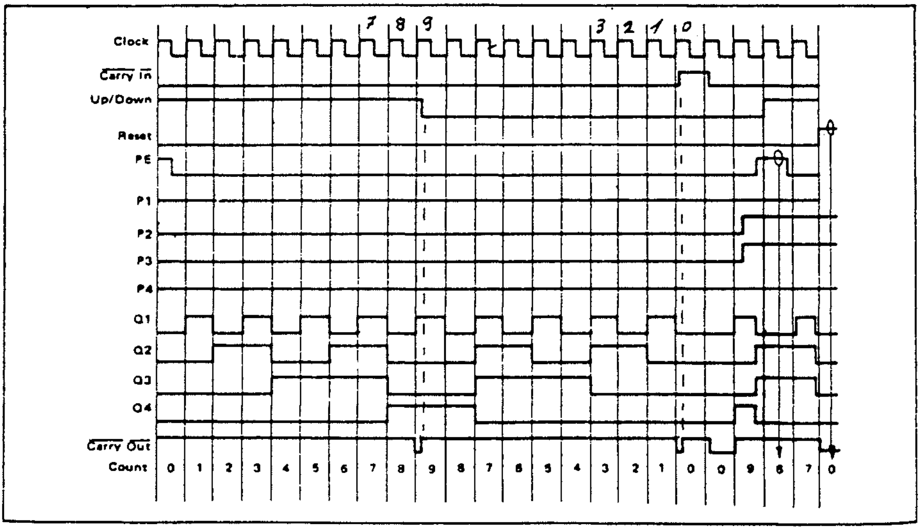




LOGIC DIAGRAM



TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	30	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8 μA/kHz) f + I_{DD}							
		15	I_T = (5.7 μA/kHz) f + I_{DD}							
		–								

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.5 ns/pF) C_L + 50 ns		5.0	–	40	80	
t_{TLH} = (0.75 ns/pF) C_L + 37.5 ns		10	–	30	60	
t_{TLH} = (0.55 ns/pF) C_L + 37.5 ns		15	–	25	50	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	–	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	–	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	–	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	–	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	–	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	–	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	–	720	1440	ns
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	–	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	–	200	400	
Blank Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 305 ns		5.0	–	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 117.5 ns		10	–	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 92.5 ns		15	–	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	–	485	970	ns
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	–	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	–	160	320	
Lamp Test Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	–	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	–	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	–	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	–	313	625	ns
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	–	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	–	90	180	
Setup Time	t_{su}	5.0	180	90	–	ns
		10	76	38	–	
		15	40	20	–	
Hold Time	t_h	5.0	0	-90	–	ns
		10	0	-38	–	
		15	0	-20	–	
Latch Enable Pulse Width	t_{WL}	5.0	520	260	–	ns

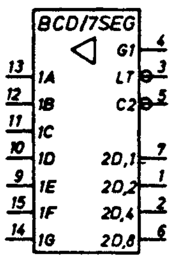
Wahrheitstabelle

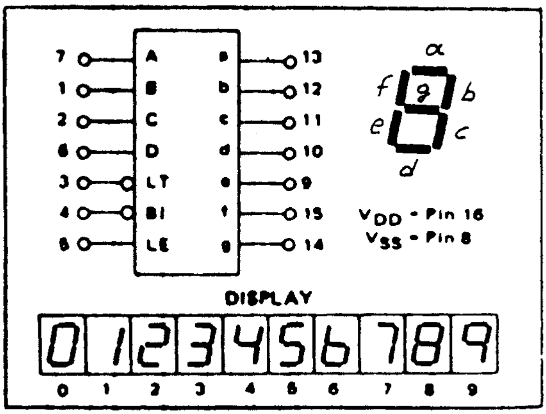
Eingänge							Ausgänge							Anzeige
C2	G1	LT	8	4	2	1	1A	1B	1C	1D	1E	1F	1G	
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	keine
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	keine
0	1	1	1	0	1	1	0	0	0	0	0	0	0	keine
0	1	1	1	1	0	0	0	0	0	0	0	0	0	keine
0	1	1	1	1	0	1	0	0	0	0	0	0	0	keine
0	1	1	1	1	1	0	0	0	0	0	0	0	0	keine
0	1	1	1	1	1	1	0	0	0	0	0	0	0	keine
1	1	1	X	X	X	X				*				*

X = Don't Care

* Abhängig vom BCD-Code, der während der 0-1-Flanke an C2 an den Addresseingängen anliegt.

Anschlußbelegung und LED-Zuordnung





ELECTRICAL CHARACTERISTICS

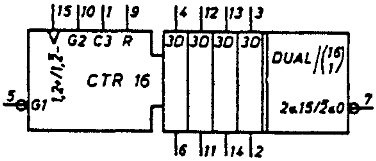
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

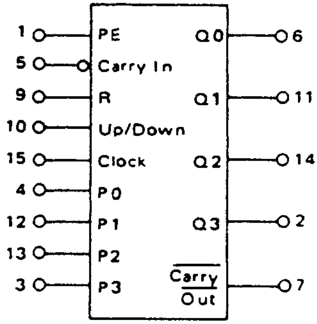
TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

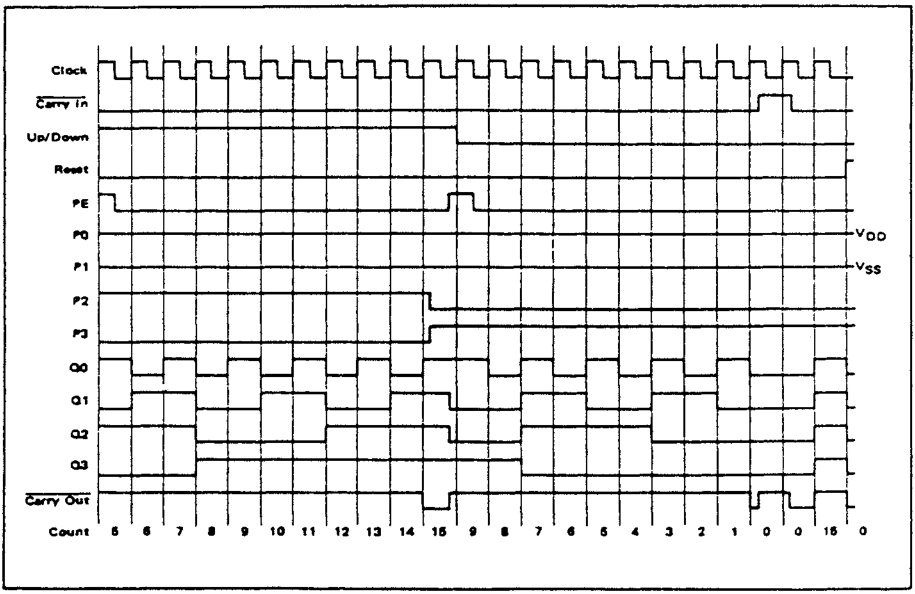
X = Don't Care

Anschlußbelegung





TIMING DIAGRAM



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

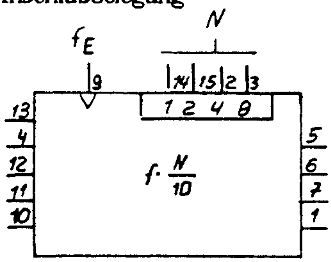
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PHL},					ns
Clock to Out	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock to Out	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 40 ns	t_{PHL}	5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Clock to E_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 210 ns	t_{PHL}	5.0	–	295	590	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
Clock to "9"	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Set or Clear to Out	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	760	
t_{PHL} = (0.66 ns/pF) C_L + 132 ns		10	–	165	330	
t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Cascade to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Strobe to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 145 ns		5.0	–	230	260	
t_{PHL} = (0.66 ns/pF) C_L + 72 ns		10	–	105	210	
t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	200	110	–	
		15	150	80	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.2	MHz
		10	–	4.5	2.5	
		15	–	6.0	3.5	
Clock Pulse Rise and Fall Time	t_{TLH},	5.0	–	–	15	µs
	t_{THL}	10	–	–	15	
		15	–	–	15	
Set or Clear Pulse Width	t_{WH}	5.0	240	80	–	ns
		10	100	35	–	
		15	75	30	–	
Set Removal Time	t_{rem}	5.0	0	-20	–	ns
		10	0	-10	–	
		15	0	-7.5	–	
Enable In Setup Time	t_{su}	5.0	400	175	–	ns
		10	150	60	–	
		15	120	45	–	

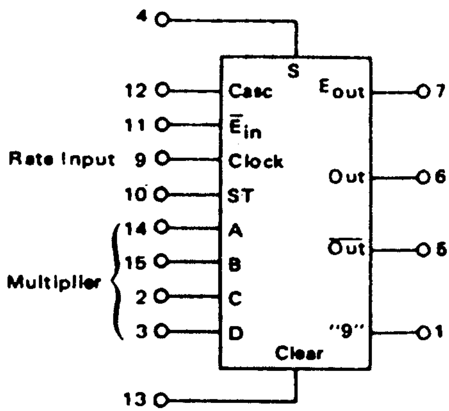
TRUTH TABLE

INPUTS										OUTPUT: NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	$\overline{E}_{in}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	0	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

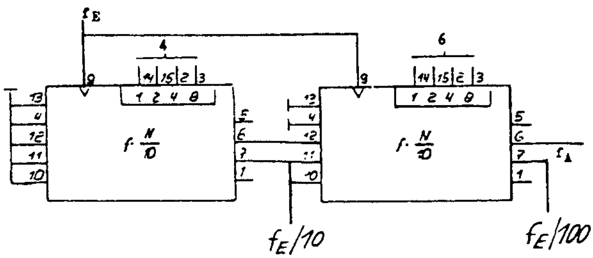
Anschlußbelegung





Beispiel

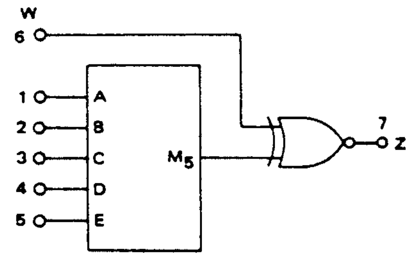
Für $N_1 = 4$, $N_2 = 6$
wird $f_A = f_E \cdot 0,46$



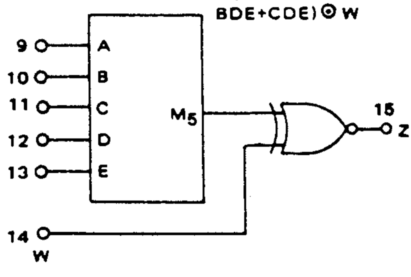
4530 Zwei Majoritäts-Gatter

SWITCHING CHARACTERISTICS* (C_L = to pF, T_A = 25°C)

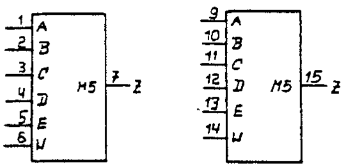
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	960	
t_{PLH} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH} = (0.5 ns/pF) C_L + 85 ns		15	–	110	300	
t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	1200	ns
t_{PHL} = (0.66 ns/pF) C_L + 162 ns		10	–	195	540	
t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 170 ns		5.0	–	255	640	
[illegible]		10	–	120	300	
t_{PLH} = (0.5 ns/pF) C_L + [illegible] ns		15	–	85	210	
t_{PHL} = (1.7 ns/pF) C_L + 195 ns	t_{PHL}	5.0	–	280	750	ns
t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	330	
t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	575	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 72 ns		10	–	105	265	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	



Z = M_5 ⊙ W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) ⊙ W



Anschlußbelegung

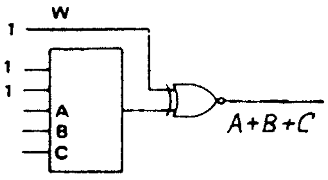


TRUTH TABLE

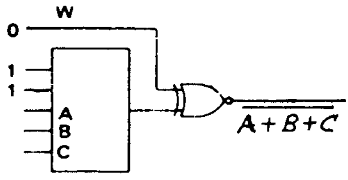
M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

⊙ ≡ Exclusive NOR ≡ $\overline{\text{Exclusive OR}}$

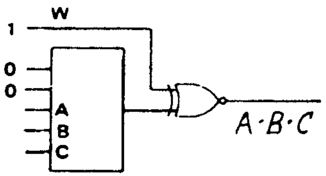
Beispiele



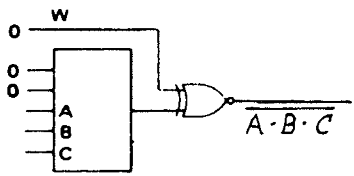
3-Input OR Gate



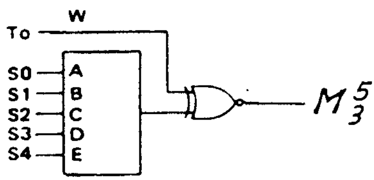
3-Input NOR Gate

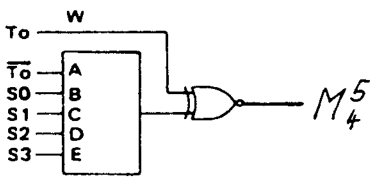


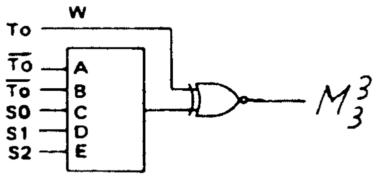
3 Input AND Gate



3-Input NAND Gate







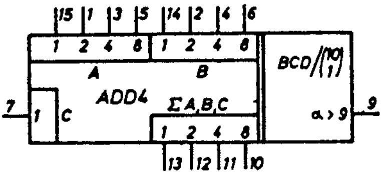
4560 BCD-Addierer
4561 Neuner-Komplement-Bildner

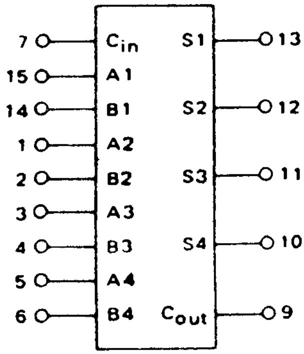
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to S						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	675	
A or B to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
C_{in} to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	450	
Turn-Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	–	800	2250	
t_{PLH} = (0.66 ns/pF) C_L + 197 ns		10	–	350	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	–	240	750	
Turn-On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	

Wahrheitstabelleund Anschlußbelegung 4560

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

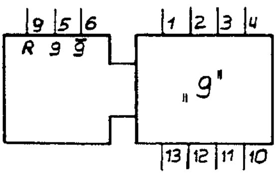


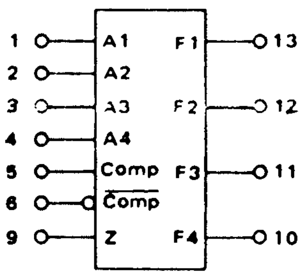


Wahrheitstabelle und Anschlußbelegung 4561

Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0					
0	0	1	A1	A2	A3	A4	Straight-through
0	1	1					
0	1	0	$\bar{A}1$	A2	$A2\bar{A}3 + \bar{A}2A3$	$\bar{A}2\bar{A}3\bar{A}4$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.





4585 4 Bit-Komparator

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	860	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	

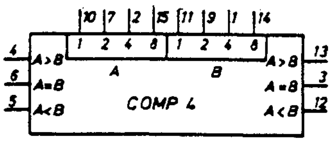
*The formula given is for the typical characteristics only.

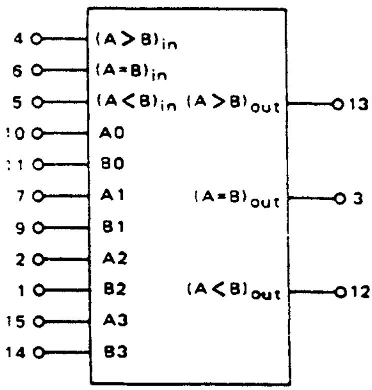
TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	1	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

Anschlußbelegung





Beispiel für einen dreidekadigen Vergleich